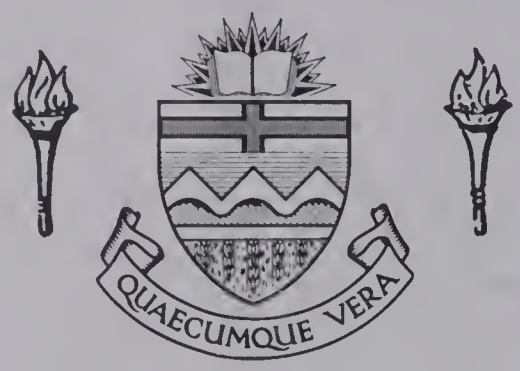

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THE UNIVERSITY OF ALBERTA

A SOLID STATE TIME DIVISION MULTIPLIER

by

© JAMES R. CONNIE

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES

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EDMONTON, ALBERTA

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UNIVERSITY OF ALBERTA

FACULTY OF GRADUATE STUDIES

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "A Solid State Time Division Multiplier" submitted by James R. Connie in partial fulfilment of the requirements for the degree of Master of Science.

ABSTRACT

This thesis involves the theory and the development of a solid state analog multiplier featuring good performance specifications at a relatively low cost.

While intended mainly for use with an analog computer, it could be used in a variety of electronic applications.

The multiplier is a four quadrant device, accepting plus and minus signals up to 10 volts at each of its two inputs and producing plus or minus signals up to 10 volts at its output. The device uses simultaneous width and amplitude modulation of a pulse train to accomplish the multiplication. The design is such that the width and amplitude modulators can be built separately for use in other projects if needed. A fundamental pulse frequency of 200 KHz is employed to produce a frequency response of 5 KHz with less than 0.5 percent distortion products remaining. The linearity of the device for A.C. signals is very good (less than 0.1 percent distortion). For D.C. signals, the output signal remains well within ±0.5 percent deviation from straight line linearity through the zero point.

A unique feature of the multiplier is the use of tunnel diode hybrid comparators in both the width and the amplitude modulators.

ACKNOWLEDGEMENTS

The writer wishes to express his appreciation for assistance received during the preparation of this work. The research described in this thesis was carried out at the University of Alberta under the supervision of Professor Y.J. Kingma, to whom the writer wishes to acknowledge his indebtedness for advice and assistance received throughout the project.

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CHAPTER 1

INTRODUCTION

In many branches of electrical engineering, electronic multipliers are in great demand. Such is the case in control system engineering.

The project for this thesis arose due to a need for an inexpensive multiplier in control systems research at the University of Alberta. They were required for use with analog computers as well as other projects. In view of the number of multipliers desired, the decision was made to develop a multiplier that would give a good compromise between performance and cost. Essentially, this is the goal of this thesis.

1.1 Choice of Method

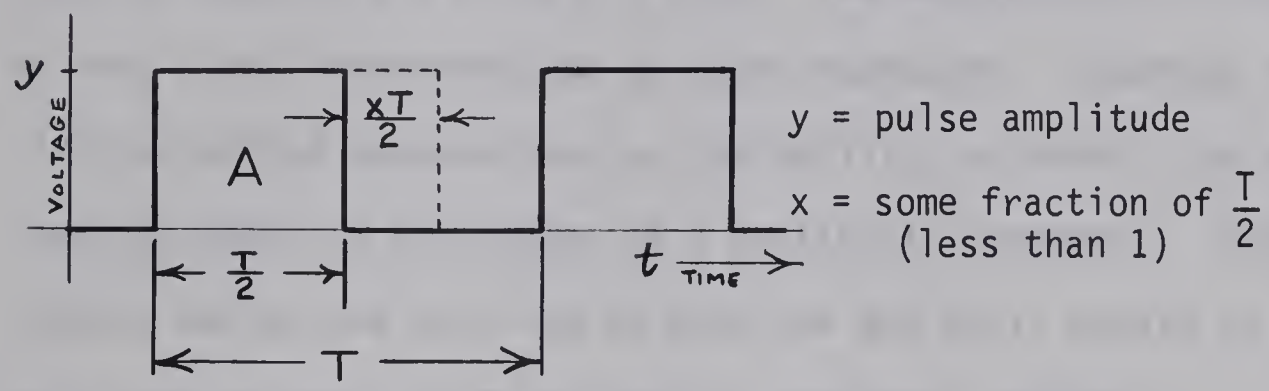
The method to be used was time division multiplication. This same method had been used in a vacuum tube multiplier circuit developed by Y.J. Kingma and J.A. Ash.[2] The idea was to use transistor circuits in a similar manner and at the same time obtain better performance.

However, experimentation soon indicated that the desired frequency response could not be obtained with the type of diode switches used by the tube multiplier. Instead, a circuit arrangement was developed using transistor switches (ie. choppers) that could operate accurately at the high repetition rates required. The basic idea of time division multiplication was retained due to several inherent advantages.

1.2 Introduction to Time Division Multiplication

This method is simply stated as the simultaneous width and amplitude modulation of a pulse train.

To illustrate very basically that this will produce true multiplication, consider the area A of a voltage pulse.



$$A = \left(\frac{T}{2} + \frac{xT}{2}\right) y = \frac{yT}{2} + \frac{xyT}{2}$$

FIG. 1.1 D.C. Width-amplitude modulated pulse train.

The average D.C. voltage of the waveform is equal to the area of the waveform divided by the period. Thus

$$V_{dc} = \frac{A}{T} = \frac{y}{2} + \frac{xy}{2} . \qquad (1\text{-}1)$$

If the term $\frac{y}{2}$ is now subtracted, the multiplication is accomplished. All that is necessary to derive V_{dc} from the waveform is a simple averaging filter. This basic process is illustrated in Fig. 1.2.

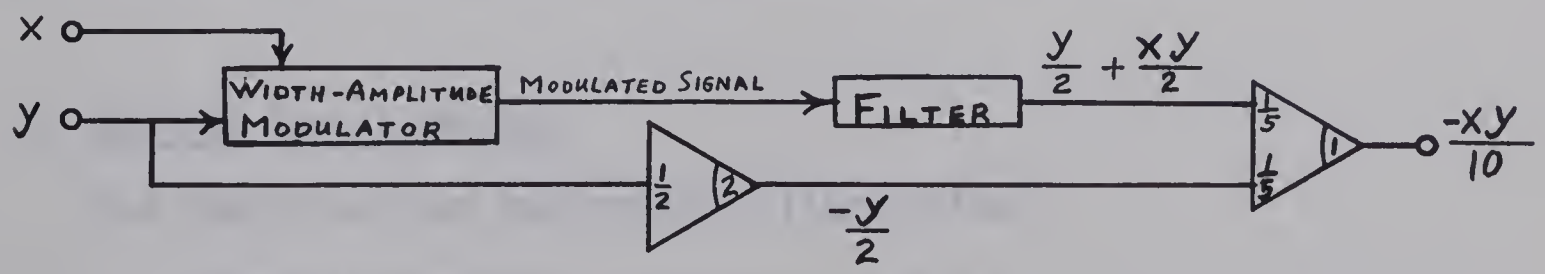
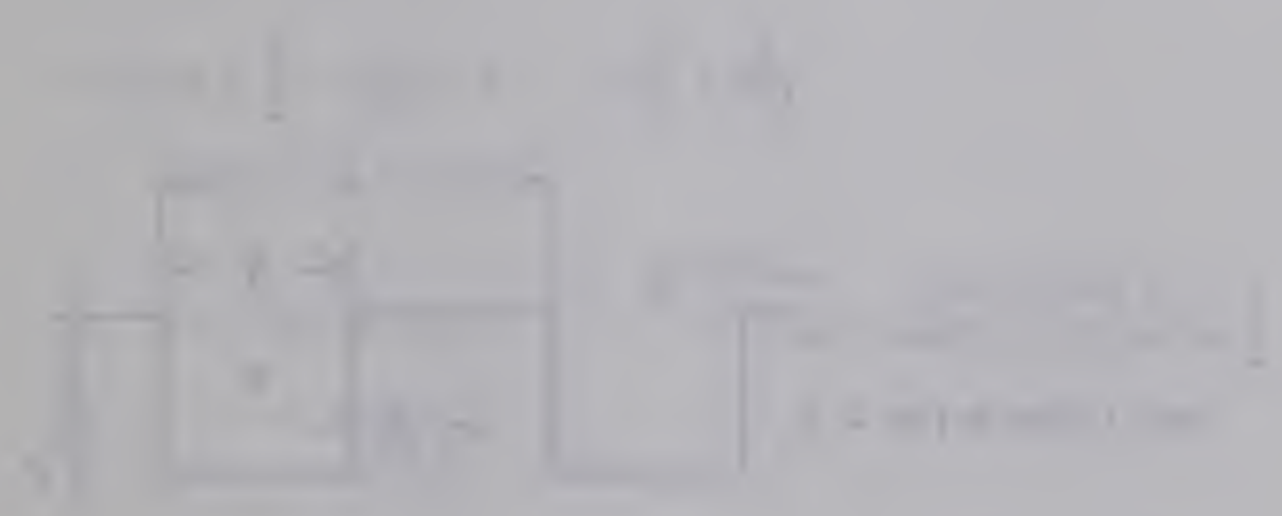


FIG. 1.2 Basic multiplier configuration.



1.3 Some Advantages and Disadvantages

The time division method of multiplication has the advantage of being able to produce very good accuracy at a low cost. Some methods like the quarter square method or the Hall-effect method depend on the accuracy of a circuit component in generating a specific transfer function such as $a = b^2$ or $E = \lambda_H iB$. The manufacture of these devices to very close tolerances can be quite expensive. Accuracy in the time division method depends more on the ability to control the waveshapes involved than the tolerances of a particular component. Thus with good circuit design the cost can be kept low and still result in a multiplier with good accuracy and a reasonable frequency response.

The main limitation to consider for this method is the frequency response. Because a low pass filter is needed to demodulate the pulse train, there is a definite limit to the frequencies that the multiplier can handle. This limit depends on what compromise can be made between the accuracy desired and the highest fundamental pulse frequency at which the waveshapes can be adequately controlled to obtain this accuracy. An additional factor that may have to be considered is how much phase shift (introduced mainly by the low pass filter) may be tolerated at the output.

The conclusion is that the final compromise will depend on which of the desired specifications are considered most important.

1.4 Desired Specifications

The specifications desired are listed below:

Overall Linearity ---------- ± 0.5 %

Frequency Response ---------- 5 KHz or more

Temperature Drift ---------- less than 2 % for 10°C

Phase Shift ---------- as small as possible

It was expected that these specifications could be met and possibly improved upon.

CHAPTER 2

OTHER MULTIPLICATION METHODS

This section is devoted to brief descriptions of some other methods used in the design and construction of multipliers. Only a few of the most popular methods were chosen to give an indication of the variety of multiplication devices available.

2.1 Quarter Square Multipliers

Multipliers of this type are among the most popular in use. They make use of a circuit component which accurately simulates a square function like $F(x) = kx^2$. To obtain the multiplication, two of these devices are used in a circuit that operates according to the following relation:

$$XY = \tfrac{1}{4}\{(X + Y)^2 - (X - Y)^2\} . \qquad (2\text{-}1)$$

Various commercial multipliers operate on this principle. The diode quarter square multiplier is one example.

(a) Diode Quarter Square Multiplier

Each square function element is constructed with a series of diodes biased such that each contributes to a small section of the total curve. A typical square element is shown in Fig. 2.1. To make a complete four quadrant multiplier, four similar elements are required as shown in Fig. 2.2. Each diode series is represented by a single diode.

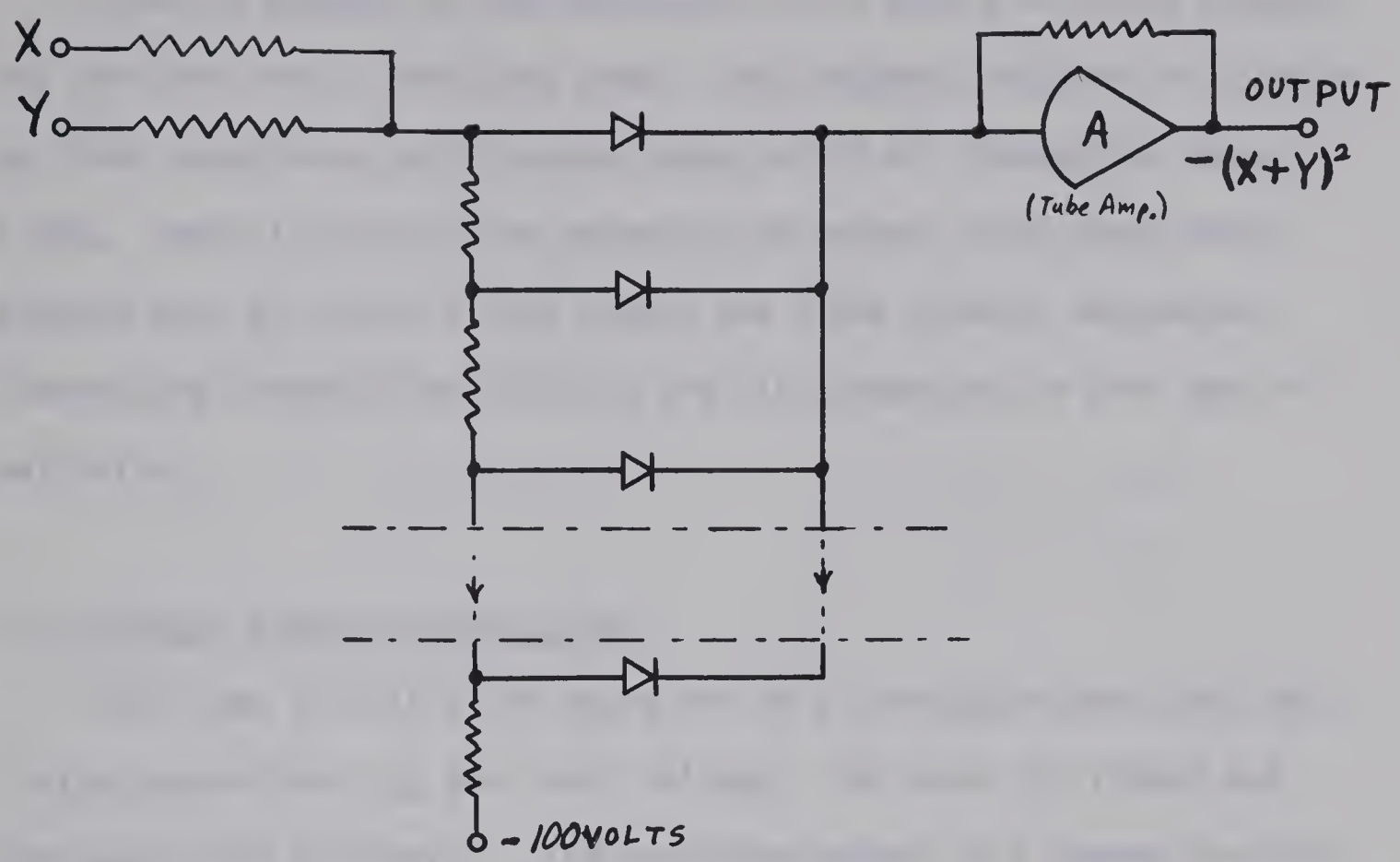


FIG. 2.1 Diode square function element.

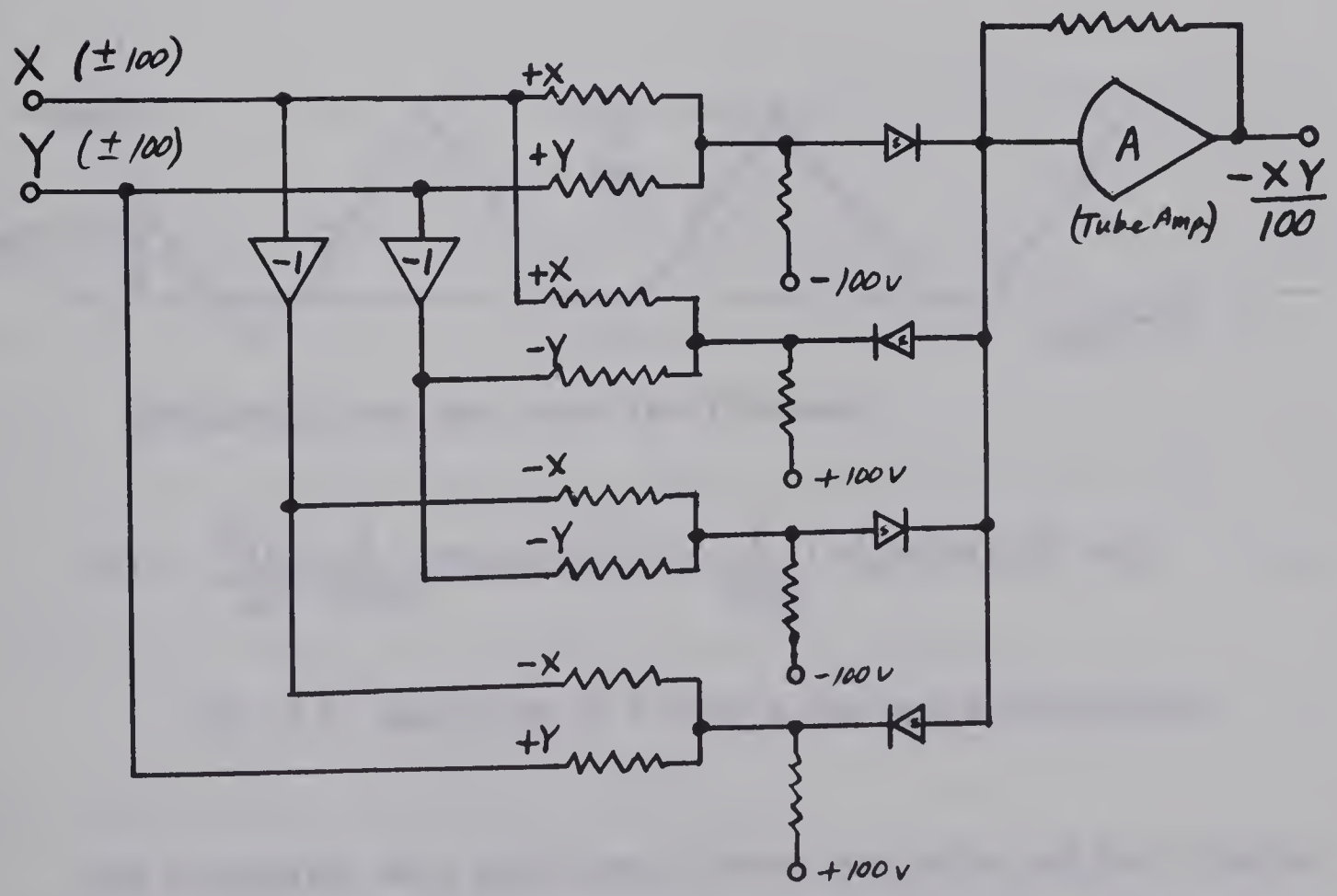
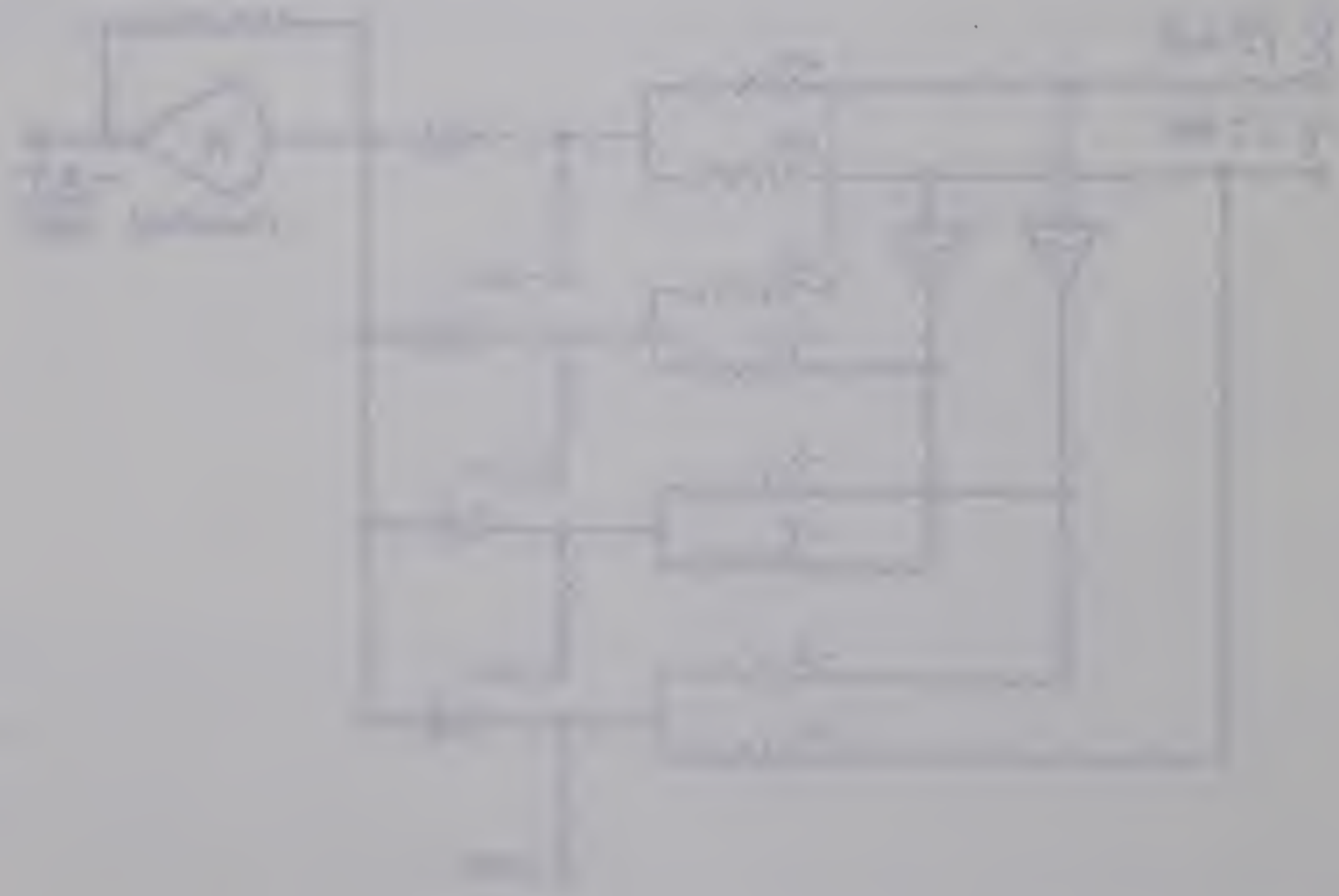


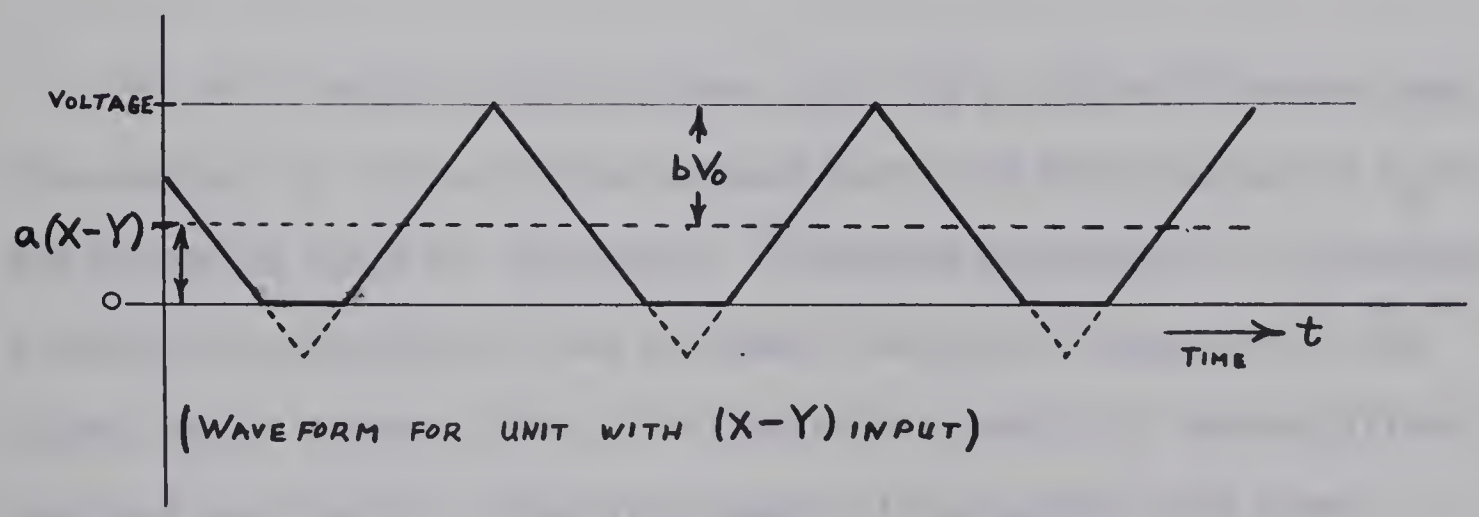
FIG. 2.2 Four quadrant diode square multiplier.



Accuracy depends on the exactness of the square function elements and the care used in matching them. The frequency response is limited by diode capacitance which causes phase shift at frequencies above 2 KHz. Special circuits are necessary to correct this phase shift problem such as circuits that reduce the diode network impedances. Temperature compensation circuits are also necessary in this type of multiplier.

(b) Triangle Averaging Multiplier

This type of multiplier makes use of a triangular wave that has a bias proportional to the input voltage. The wave is clipped and averaged (with a filter) . The resulting output is a square function of the input voltage. Two of these units connected according to equation (2-1) result in the expression shown in Fig. 2.3.



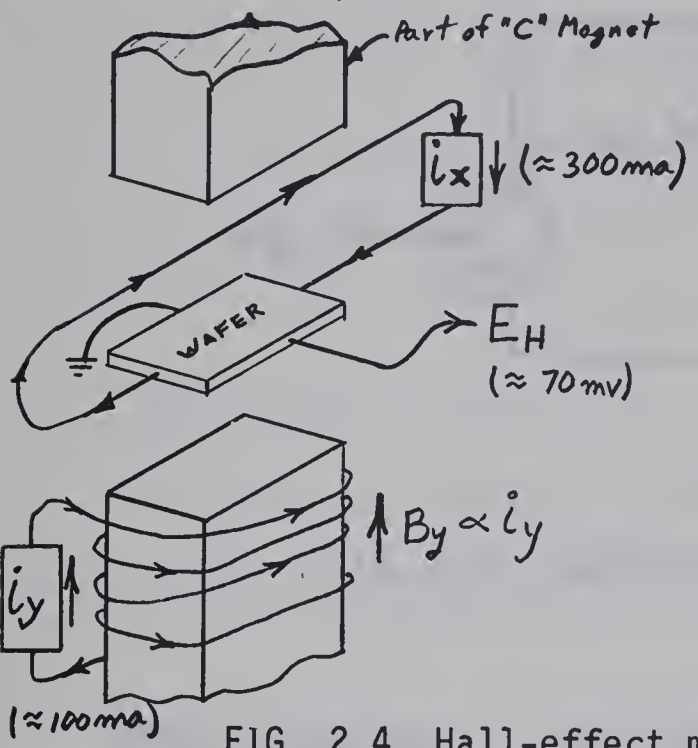
$$kXY = \frac{-kbV_0}{a^2}\left\{\frac{1}{4bV_0}\{bV_0+a(X-Y)\}^2 - \frac{1}{4bV_0}\{bV_0+a(X+Y)\}^2 - aY\right\}$$

FIG. 2.3 Operation of Triangle Averaging Multiplier.

The triangular wave amplitude V_0 must be stable and the clipping of the wave must be done accurately to obtain good performance.

2.2 Hall-effect Multiplier (8,9)

This multiplier is based on the formula describing an effect present in certain suitable semiconductor wafers such as indium arsenide and doped silicon. The formula is given in Fig. 2.4 which shows the multiplier.



$$E_H = \lambda_H \, i \, B$$

E_H = output voltage

λ_H = semiconductor constant

B = magnetic flux density

H = magnetic field strength

$$B \propto i_{coil}$$

Thus $B = k \, i_y$

and $E_H = (\lambda_H k) \, i_x \, i_y$

FIG. 2.4 Hall-effect multiplier.

For thin indium arsenide wafers, $\lambda_H \simeq 50$ to 100 mv/Kilogauss-amp. The accuracy of the multiplier depends partly on the accuracy of λ_H in the operating range of the device. A problem encountered in constructing a practical multiplier is the extremely low source impedance of the output signal (about 1 ohm). This makes the design of the amplifiers required very exotic. Specially doped silicon wafers have given reasonable compromises between λ_H and source impedance. The frequency response is limited to a few KHz by the electromagnet.

2.3 Field Effect Transistor Multipliers

The development of the field effect transistor resulted in a relatively new method of multiplication. The multiplication is based

on the proportionality between the channel conductance and the gate voltage. The circuit shown in Fig. 2.5 illustrates a simple two transistor FET multiplier.(13)

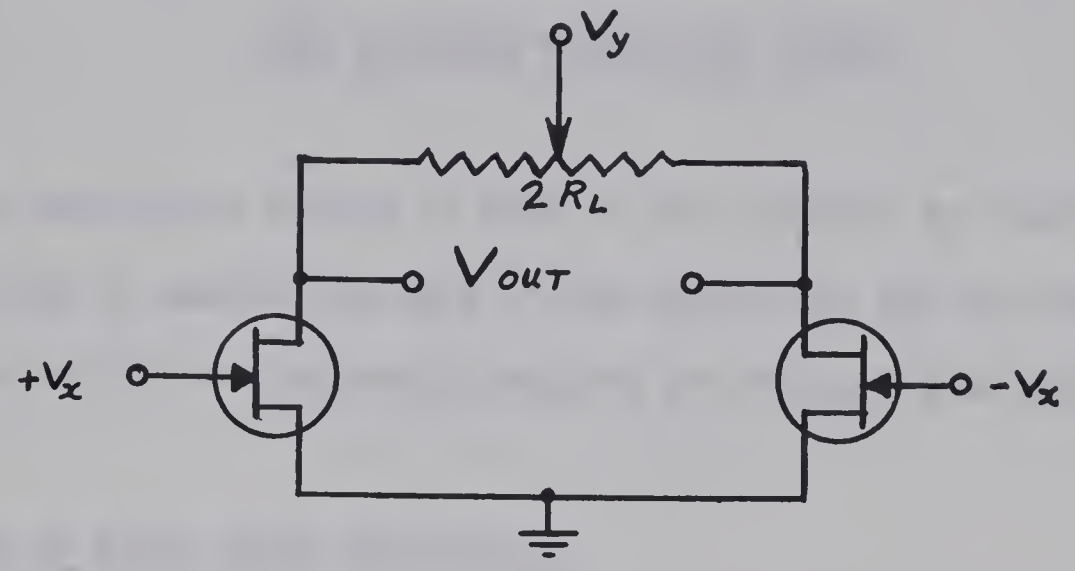


FIG. 2.5 Dual FET multiplier.

One voltage input is applied with opposite polarity to the gates. The other voltage input is applied to the two channels. The difficulties involved with constructing a workable multiplier include the necessity to select FET's that are matched as well as chosen for their temperature drift characteristics. The input voltages must be kept small to avoid nonlinearity, and the resulting output voltages are also small. The circuit is said to be linear within a few percent with these restrictions but the frequency response is quite high (about 200 KHz). The response is limited mainly by the capacitance between the gate and the channel of the FET's.

Other applications of FET's are being made(14) and they are among the most promising devices for future multiplier designs.

This chapter has described just a few of the large variety of multipliers available,(17) and the future promises many more.

CHAPTER 3

TIME DIVISION MULTIPLIER THEORY

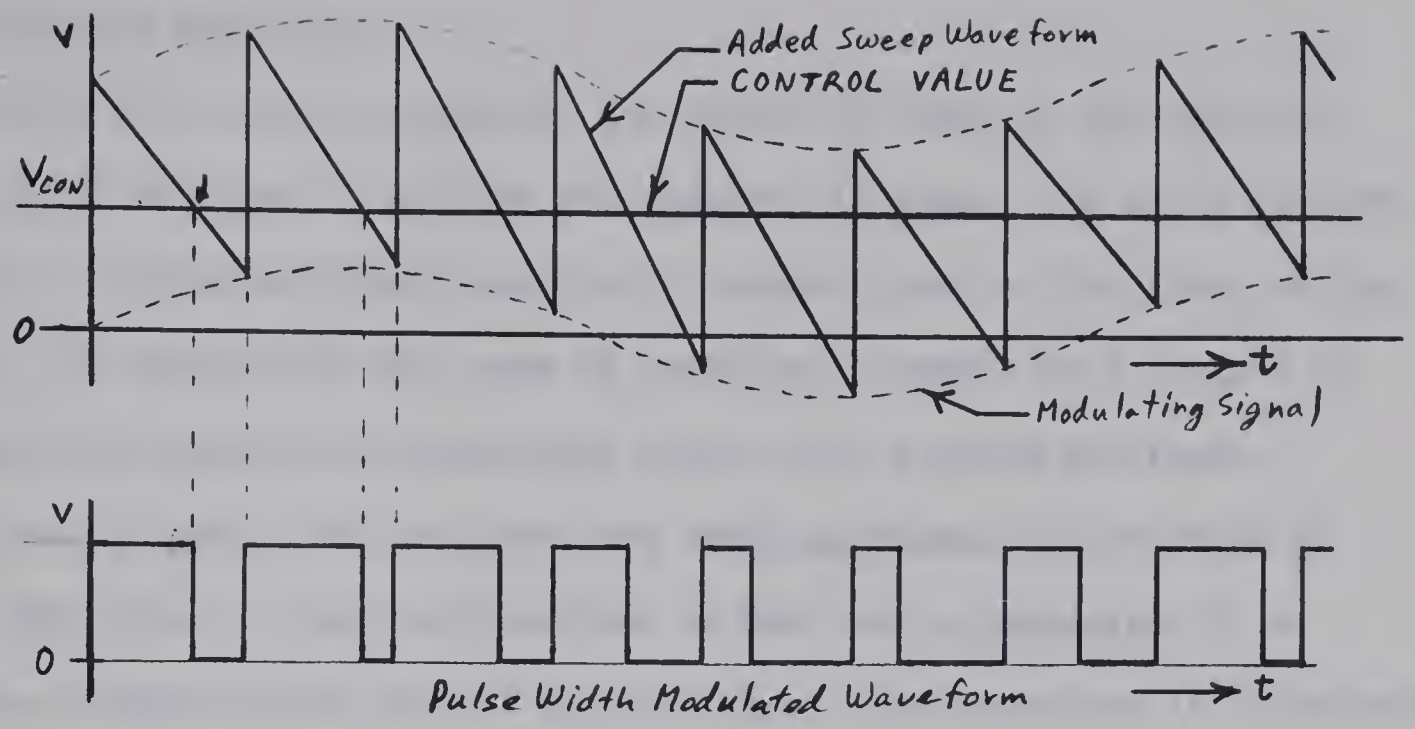
Pulse modulation theory is used in this section to show the specific type of modulation used in the multiplier and to investigate in greater detail the frequency spectrum of the modulated waveform.

3.1 Types of Pulse Width Modulation

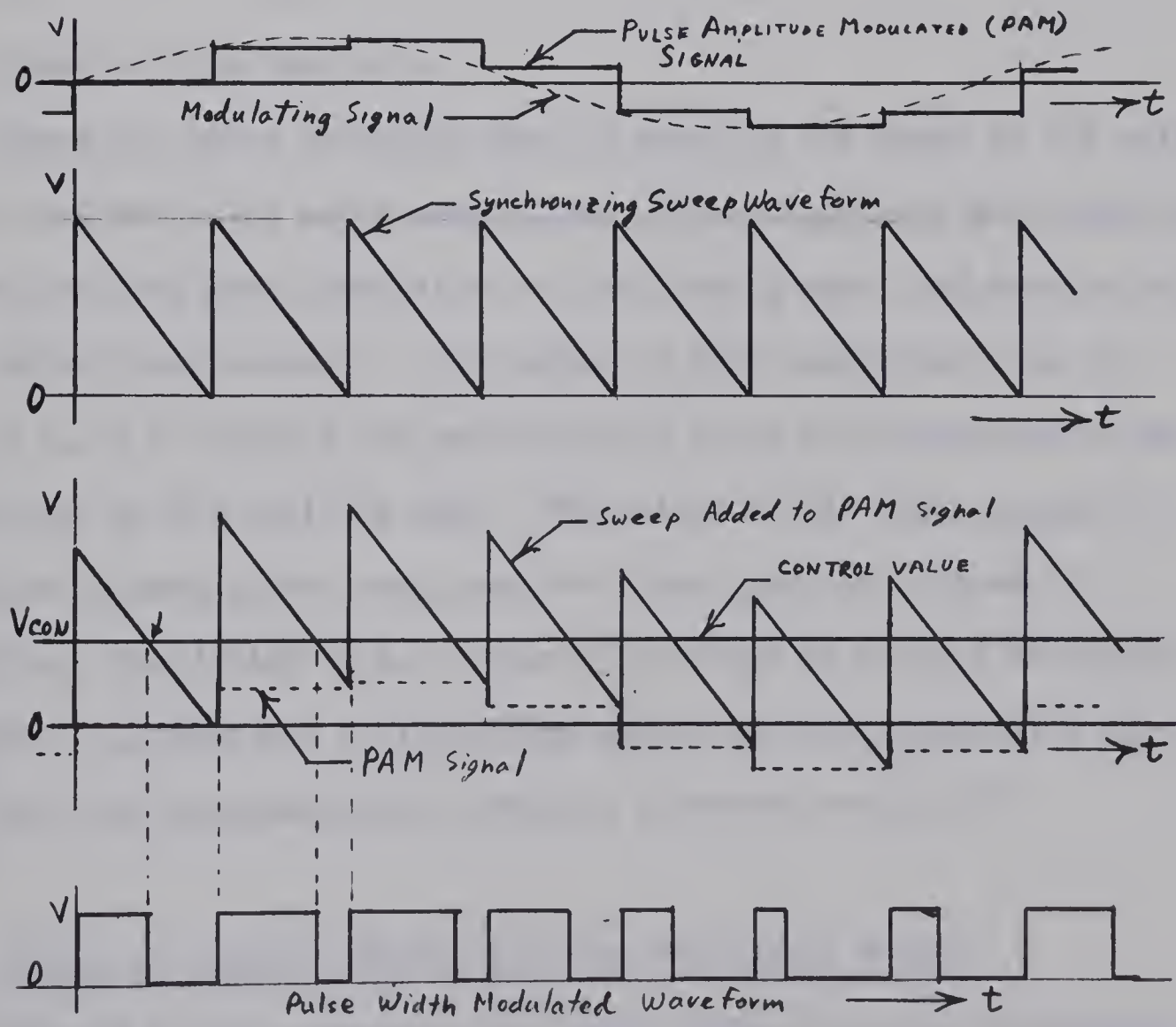
There are two different methods of sampling the modulation waveform which result in two basic types of width modulation.

(a) Natural Sampling

The simplest method of producing width modulated pulses is by the use of natural sampling. With this method of sampling the start of the pulse occurs at regular intervals corresponding to the fundamental pulse frequency f_s. However, the end of the pulse is controlled by the value of the signal at that instant. Thus, the sampling of the modulating signal occurs at different times within the pulse frequency period. This is nonuniform sampling and is called natural sampling. This type of sampling is produced by adding a sweep waveform (operating at the fundamental pulse frequency) to the modulating waveform and feeding the result into a comparator as shown in Fig. 3.1(a). The comparator turns the pulse ON and OFF according to whether the input signal is above or below the control value of the comparator.

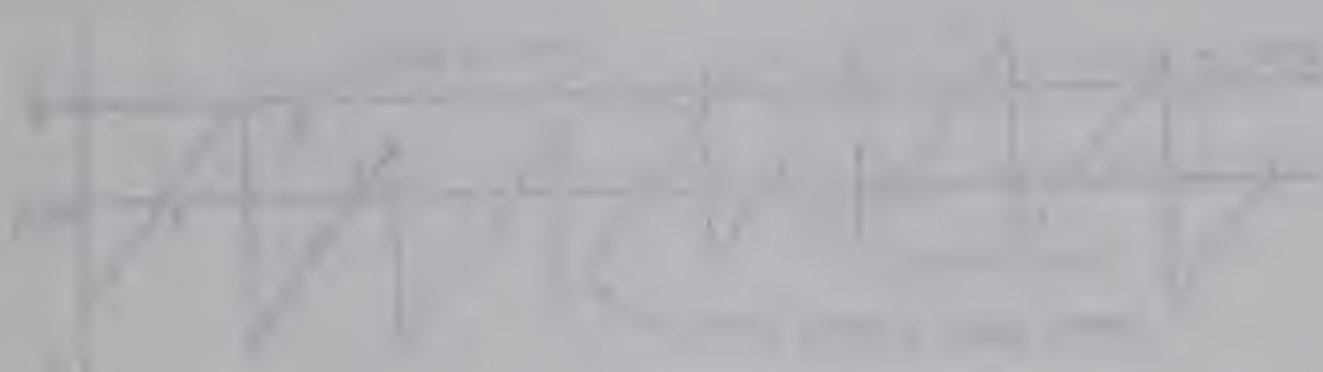


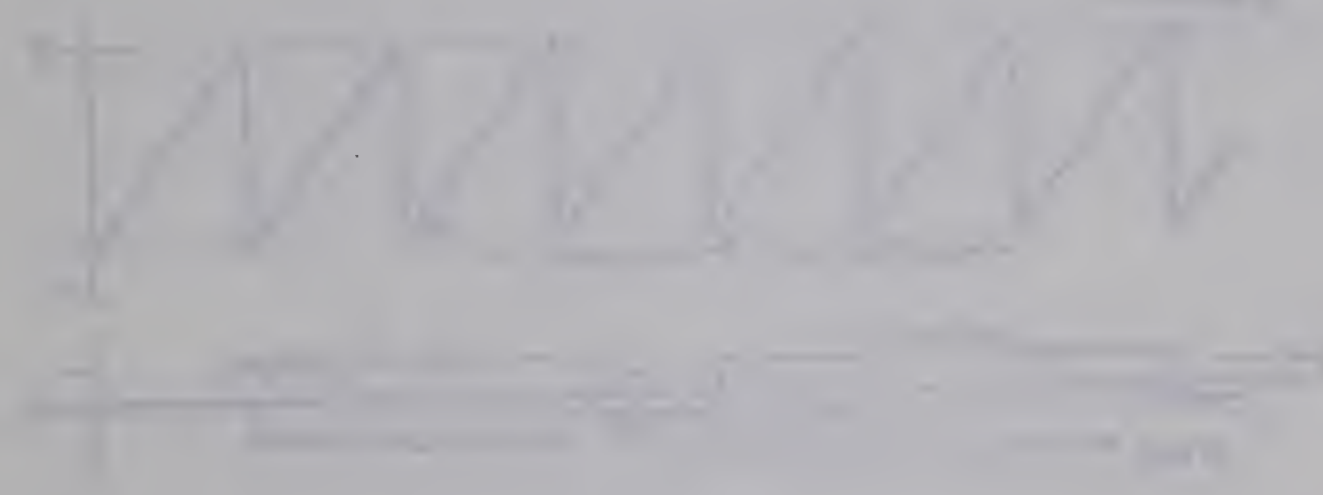
(a) Natural sampling.



(b) Uniform sampling.

FIG. 3.1 Generation of pulse width modulation.





(b) Uniform Sampling

With this type of sampling, the sample is taken at the start of each pulse and thus is uniform with respect to time. The width of each pulse is then made proportional to the sample taken at the start of the pulse. To accomplish this type of sampling, a sample hold circuit is required to convert the modulating signal into a pulse amplitude modulated signal. The synchronizing sweep waveform is then added to this PAM signal. The total waveform is fed into a comparator in a similar manner to the natural sampling case. The procedure is illustrated by Fig. 3.1(b).

(c) Types of Edge Modulation

There are three different ways to modulate the edges of the pulse train used for pulse width modulation. These three ways are: modulation of the trailing edge, modulation of the leading edge, and modulation of both edges simultaneously. The method of edge modulation used in Fig. 3.1, to illustrate the generation of pulse width modulation, was modulation of the trailing edge. Modulation of the leading edge is produced by making the sweep waveform slope positive instead of negative. Modulation of both edges is produced by using a triangular waveform. Leading and trailing edge modulation are essentially the same but dual edge modulation produces different results.[1]

(d) Choice of Sampling Method and Edge Modulation Method

Because of the components that were eventually used to generate the sweep waveform, trailing edge modulation became the most convenient method to use in the pulse width modulator section of the multiplier.

Natural sampling was chosen for use in the multiplier because of its simplicity and because uniform sampling basically produces an undesirable output. Black[1] shows that natural sampling results in a frequency spectrum containing the modulating signal f_x, the fundamental pulse frequency f_s and harmonics of f_s, and sideband frequencies about these f_s frequencies at multiples of f_x away. Filtering of the higher frequency components leaves just f_x. However, when uniform sampling is used, there are harmonic frequencies of the modulation signal f_x produced in addition to the previously mentioned components. In this case, unless f_x is fixed, proper filtering of the output is difficult and thus uniform sampling is considered unsuitable for this application.

3.3 Analysis of Time Division Multiplication

This section is devoted to mathematical analysis of the simultaneous width-amplitude modulated waveform that the multiplier operation is based on. The simple case for multiplication of D.C. signals was illustrated in section 1.2. This section is devoted to the more general case where the sum of the frequencies of the input signals can range from D.C. to one half of the sampling frequency. The analysis of the pulse width modulated waveform has already been done in the literature.[1] This result is modified to include the pulse amplitude modulation as used in the time division multiplier.

(a) Mathematical Analysis

The expression obtained for a width modulated pulse train by Black in his book "Modulation Theory" is shown in eq. (3.1) in a slightly modified form. This expression includes the pulse amplitude term H

whereas Black assumed H to be unity in his expression (eq. 17-25 on page 275 of "Modulation Theory"). However, eq. (3.1) is written to include H in the proper positions.

$$F_x(t) = kH + \frac{MH}{2}\cos\omega_x t + \sum_{m=1}^{m=\infty} H\,\frac{\sin m\omega_s t}{m\pi}$$

$$- \sum_{m=1}^{m=\infty} H\,\frac{J_o(m\pi M)}{m\pi}\sin(m\omega_s t - 2m\pi k)$$

$$- \sum_{m=1}^{m=\infty}\sum_{n=\pm 1}^{n=\pm\infty} H\,\frac{J_n(m\pi M)}{m\pi}\sin(m\omega_s t + n\omega_x t - 2m\pi k - \frac{n\pi}{2}) \qquad (3\text{-}1)$$

where

M = modulation index (ie. ratio --- $\frac{\text{total pulse width change}}{\text{pulse period}}$)

k = ratio of quiescent PW to PP (normally 0.5)

H = pulse amplitude

$J_n(n\pi M)$ = Bessel function of $(n\pi M)$

Modulating signal (x input) = $M\cos\omega_x t$.

The derivation of eq. (3-1) by Black assumes that H is a constant. However, H can become an independent variable (eg. H = y input) without affecting the validity of eq. (3-1). This is true because the variable in H is independent of the variables of integration in any integrals that H appears in. Thus eq. (3-1) can be used in the analysis of the multiplier waveform. The frequency spectrum represented by eq. (3-1) is illustrated in Fig. 3.2(a).

An expression for the width-amplitude modulated waveform of the multiplier can now be written.

The x and y inputs are written as

$$x(t) = M \cos \omega_x t \qquad \text{(width modulation)}$$

$$y(t) = H = Y \cos (\omega_y t + \theta_y) \qquad \text{(amplitude modulation).} \quad (3\text{-}2)$$

Substitute eq. (3-2) into eq. (3-1) to get

$$F_{xy}(t) = kY \cos (\omega_y t + \theta_y) + \frac{MY}{2} \cos \omega_x t \cos (\omega_y t + \theta_y)$$

$$+ \sum_{m=1}^{m=\infty} \frac{Y}{m\pi} \sin m\omega_s t \cos (\omega_y t + \theta_y)$$

$$- \sum_{m=1}^{m=\infty} \frac{YJ_o(m\pi M)}{m\pi} \sin (m\omega_s t - 2m\pi k) \cos (\omega_y t + \theta_y)$$

$$- \sum_{m=1}^{m=\infty} \sum_{n=\pm 1}^{n=\pm\infty} \frac{YJ_o(m\pi M)}{m\pi} \{\sin(m\omega_s t + n\omega_x t - 2m\pi k - \frac{n\pi}{2})$$

$$\times \cos (\omega_y t + \theta_y)\}. \quad (3\text{-}3)$$

The resulting expression essentially corresponds to amplitude modulating each frequency term of eq. (3-1). The result is: a residual A.C. signal, the desired multiplication, and high frequency distortion terms. In simple form, eq. (3-3) can be written as

$$F_{xy}(t) = ky(t) + \frac{x(t)y(t)}{2} + \Sigma \text{ (Distortion Frequencies).}$$

If the signal is filtered and k is made the normal value of 0.5 (for a 50 percent duty cycle in the quiescent state), then the expression becomes

$$F_{xy}(t) = \frac{y(t)}{2} + \frac{x(t)y(t)}{2} . \qquad (3\text{-}4)$$

The expression of eq. (3-4) agrees with the result obtained in the case

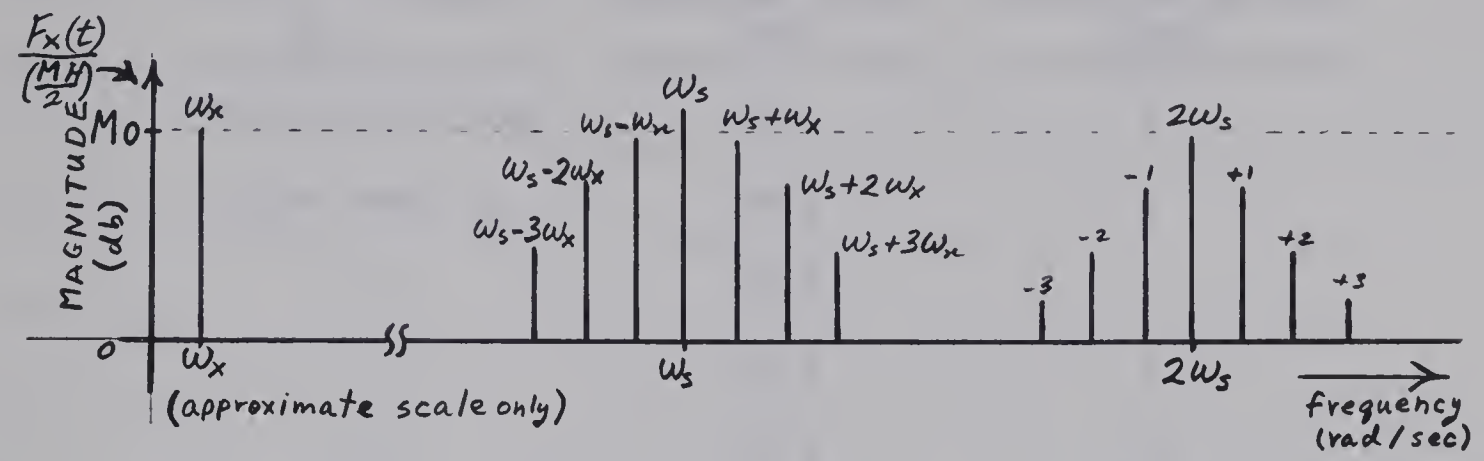
for D.C. signals in section 1.2 (eq. (1-1). However, assuming proper filtering, it is valid for A.C. signals as well as D.C. signals.

To obtain an expression that will give the frquency spectrum of the width-amplitude modulated wave, eq. (3-3) can be expanded and rearranged to give

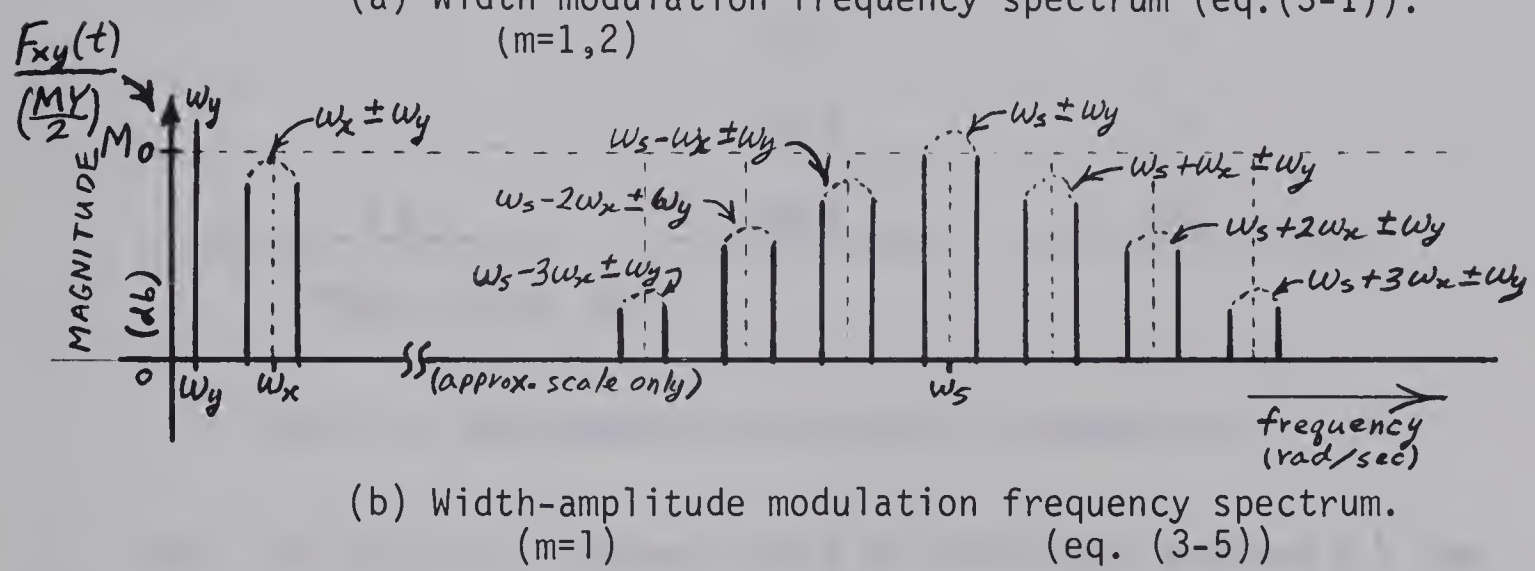
$$
\begin{aligned}
F_{xy}(t) = kY \cos(\omega_y t + \theta_y) \; + \; & \frac{MY}{4}\{\cos\{(\omega_x+\omega_y)t + \theta_y\} \\
& + \cos\{(\omega_x-\omega_y)t - \theta_y\}\} \\
+ \sum_{m=1}^{m=\infty} & \frac{Y}{2m\pi}\{\sin\{(m\omega_s+\omega_y)t + \theta_y\} + \sin\{(m\omega_s-\omega_y)t - \theta_y\}\} \\
- \sum_{m=1}^{m=\infty} & \frac{YJ_0(m\pi M)}{2m\pi}\{\sin\{(m\omega_s+\omega_y)t + \theta_y - 2m\pi k\} \\
& + \sin\{(m\omega_s-\omega_y)t - \theta_y - 2m\pi k\}\} \\
- \sum_{m=1}^{m=\infty} \sum_{n=\pm 1}^{n=\pm\infty} & \frac{YJ_n(m\pi M)}{2m\pi}\{\sin\{(m\omega_s+n\omega_x+\omega_y)t + \theta_y - 2m\pi k - \frac{n\pi}{2}\} \\
& + \sin\{(m\omega_s+n\omega_x-\omega_y)t - \theta_y - 2m\pi k - \frac{n\pi}{2}\}\}.
\end{aligned}
\tag{3-5}
$$

As can be seen in eq. (3-5), the result of introducing amplitude modulation to a width modulated pulse train is a modification of the frequency spectrum. In the new spectrum (shown in Fig. 3.2(b)), each of the previous frequency components is replaced by two components of one half the magnitude. The positions of the new frequency components are $\pm\omega_y$ from the original positions. In addition, a residual frequency component is produced at ω_y. When the wave is properly demodulated by a filter, the frequency spectrum at the output will contain this undesired residual component at ω_y as well as the desired frequency components $|\omega_x + \omega_y|$ and $|\omega_x - \omega_y|$. The latter components represent

the signal arising from the multiplication of the x and y signals. Measures to eliminate the unwanted ω_y component are discussed in chapter 4.



(a) Width modulation frequency spectrum (eq.(3-1)). (m=1,2)



(b) Width-amplitude modulation frequency spectrum. (m=1) (eq. (3-5))

FIG. 3.2 Modulation frequency spectrums. (n=±1 to n=±3)

(b) Magnitude of Distortion Frequency Components

To get an idea of the magnitude of the distortion frequency components produced, some of the components of the frequency spectrum for width modulated pulses were computed. Measurements were also taken from a working width modulator to check with the computations. A table of values for the frequency components is shown in Fig. 3.3. Some of the measured values are not tabulated because the frequency analyzer used had a limited range of measurement (up to 50 KHz only). The computations and measurements were based on values of k=0.5, M=0.5, m=1, and n=±1 to n=±6. The values in the table are referred to a

modulation signal value of 0 db.

No. of Sideband (n)	Computed Values (db)	Measured Values (db)
Modulation Freq.	0	0
Pulse Freq. ω_s	+5.5	↓
± 1	-2.8	↓
± 2	-10.0	↓
± 3	-21.1	-19
± 4	-35.0	-31
± 5	-50.9	-46
± 6	-66.0	-67

M=0.5, k=0.5, m=1.

FIG. 3.3 Magnitudes of distortion frequencies.

Only the first six sidebands need be considered because all the higher order sidebands are too small to be of interest. The disagreement between the measured and the computed values could be partly due to errors in measurement and partly due to the effects of voltage spikes on the width modulator waveform or to other imperfections of the wave.

3.3 Demodulation of the Width-Amplitude Modulated Waveform

Knowledge of the frequency spectrum makes proper design of the demodulating filter easier. If an upper limit is put on the sum of the two modulation frequencies (ie. $f_x + f_y \leq 5$ KHz), examination of equations (3-1) and (3-5) shows that the worst distortion condition will occur for pure width modulation. Thus a filter suitable for

demodulating a width modulated waveform will also be suitable as a demodulator for the multiplier. The table of Fig. 3.2 shows that the sideband frequency components become insignifigant from the sixth component and higher. Thus a suitable filter must supply a minimum of 55 db of attenuation at the pulse frequency (200 KHz) and still supply some attenuation six sidebands lower. The rate of attenuation of a third order Butterworth filter (60 db per decade) was found to be suitable to provide the filtering required without excessive phase shift in the band-pass region of the filter. With this filter, a cutoff frequency f_c of 22 KHz will result in about 0.3 percent distortion due to the 200 KHz pulse frequency. Modulation frequencies up to 20 KHz will not result in extra distortion. A better result can be obtained by choosing the cutoff frequency to be 15 KHz. This will attenuate the pulse frequency component by about 65 db resulting in about 0.1 percent distortion or less. Modulation frequencies up to 15 KHz are still theoretically possible. The design of the filter is shown in detail in section 5-8.

This chapter has shown that a multiplier operating at a sampling frequency of f_s = 200 KHz can theoretically produce output frequencies of up to 15 KHz with negligible distortion. However, due to the amount of phase shift in the output at these frequencies, the multiplier was ultimately rated for operation of up to 5 KHz only.

CHAPTER 4

DEVELOPMENT OF PRACTICAL CIRCUIT CONFIGURATIONS

As seen in the previous chapter, a width-amplitude modulated train of positive pulses can be represented by an equation of the form

$$F_{xy}(t) = k_1 y(t) + k_2 x(t)y(t) + \Sigma \text{ (high frequency distortion terms).}$$

If the signal is passed through a suitable low pass filter the remaining terms are

$$F_{xy}(t) = k_1 y(t) + k_2 x(t)y(t) .$$

There is an obvious need to eliminate the residual $k_1 y(t)$ term in order to obtain a proper multiplier output. Various possible circuit configurations for accomplishing this elimination are discussed in this chapter.

4.1 Systems Using Double Polarity Choppers

A double polarity chopper has the capability of chopping either a positive or negative voltage to a zero reference. Thus it can be used to produce a pulse train where the amplitude y(t) can vary sinusoidally about zero as shown in Fig. 4.1.

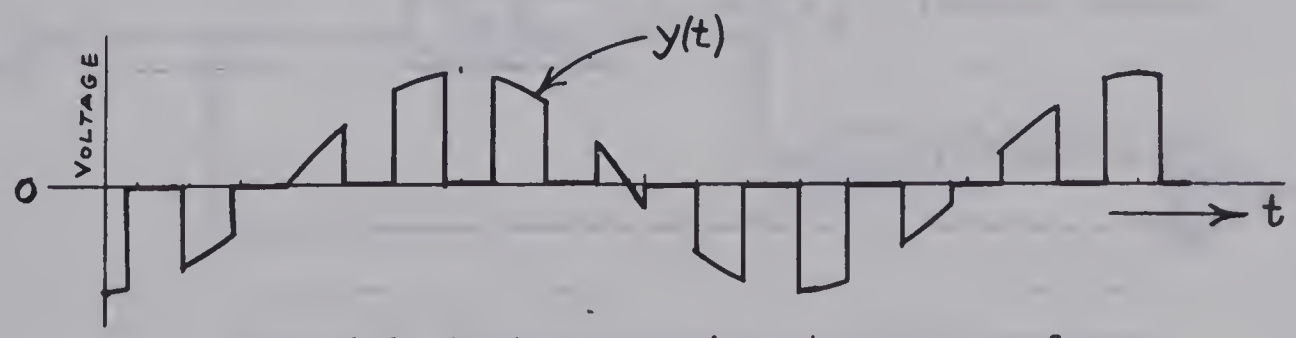
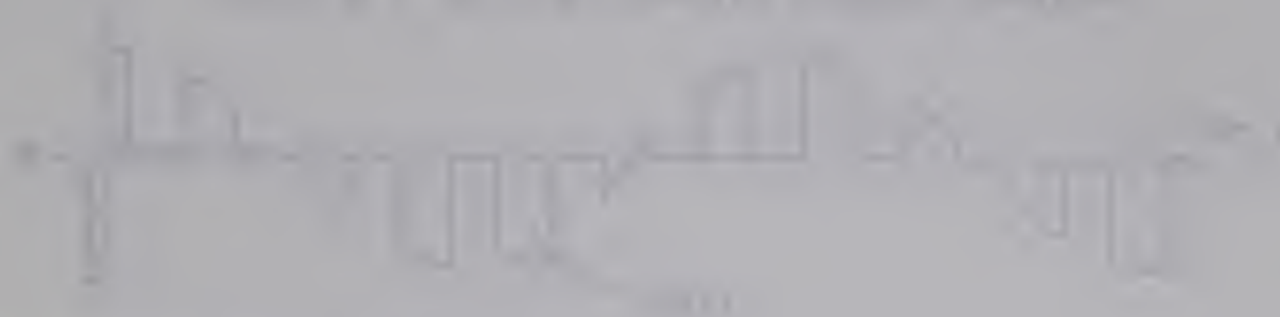


FIG. 4.1 Double polarity chopper waveform.



A variety of configurations using this chopper are possible. Some are better than others but are more complicated. However, the systems are generally simpler with this chopper than with the single polarity chopper discussed later in this chapter.

(a) Direct Method - using only one chopper.

This method (illustrated in Fig. 4.2) subtracts the $k_1y(t)$ term directly from the demodulated signal at the filter output. The modulated pulse train is produced by using a pulse width modulator to control the duty cycle of the chopper which in turn amplitude modulates the y(t) signal. The polarity inversion in the filter can be produced by the use of an active filter (which uses an inverting operational amplifier) or by the use of an inverting amplifier with a passive filter. Another operational amplifier acts as a summer and with the proper gains, produces the desired output; $\frac{x(t)y(t)}{10}$. The attenuation of xy by a factor of 10 is necessary to prevent the multiplier output from being a much larger voltage than the input voltages. To illustrate: if x(t) = 10 volts and y(t) = 10 volts, then x(t)y(t) would be 100 volts which is unreasonable for transistor circuits. A value of $\frac{xy}{10}$ = 10 volts is much more sensible.

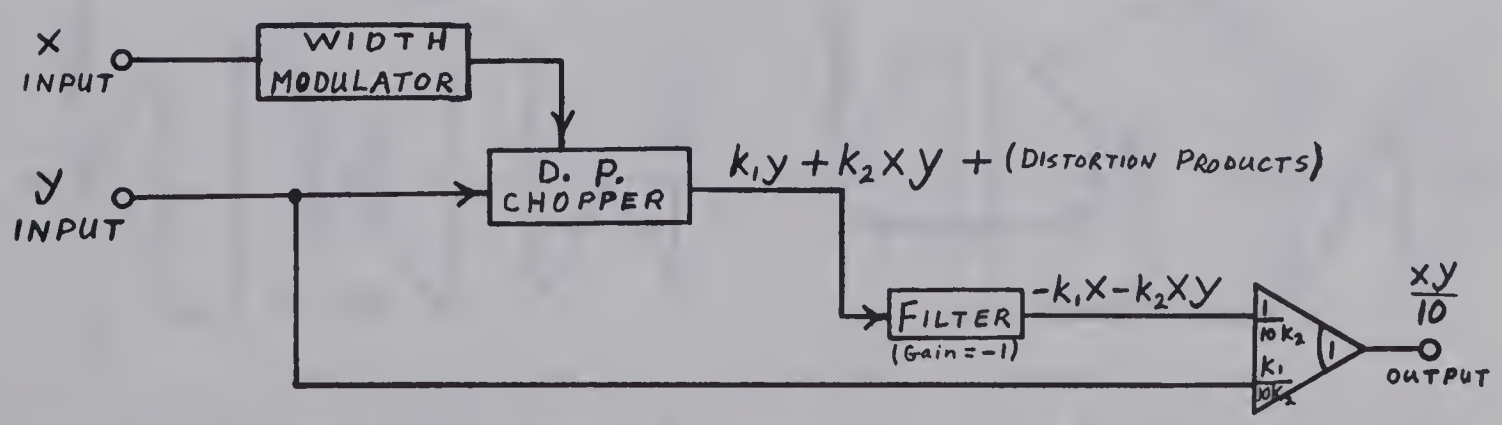


FIG. 4.2 Direct method use of D.P. chopper.

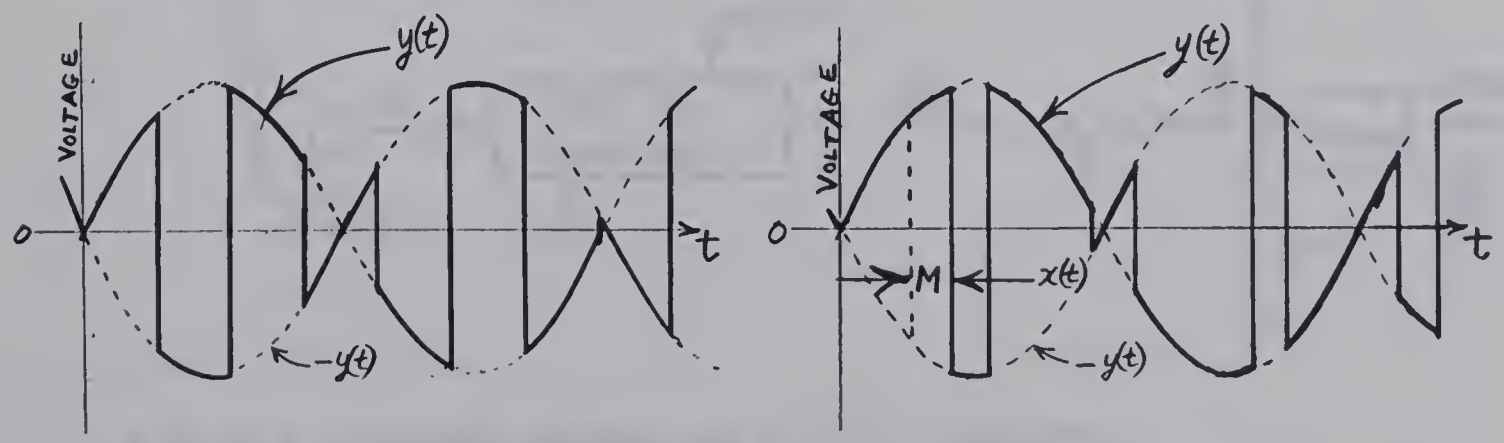
There are some disadvantages to using this method. The main objection arises from the phase shift of the $k_1 y(t)$ term after demodulation by the filter. This occurs at higher frequencies where the phase shift of the filter starts to take effect. Because of the phase shift of the $k_1 y(t)$ term with respect to the input $y(t)$, proper subtraction cannot take place in the output amplifier resulting in an undesirable residual signal.

A possible solution could be to put the $y(t)$ signal through another filter with similar phase shift characteristics before using it to cancel out the $k_1 y(t)$ residual signal. However, the difficulties of matching the two filters to a tolerance close enough to be effective make this impractical.

With work, this problem might be overcome. However, the indirect method discussed next is more promising.

(b) Indirect Method - using two choppers.

A study of the problem revealed that the $k_1 y$ component could be removed before filtering by a suitable alteration of the chopped waveform. If the chopper is operated so that it chops from +y to -y instead of from just +y to zero, the waveforms in Fig. 4.3 result.



(a) $x(t) = 0$, $y(t) = \sin \omega_y t$ (b) $x(t) = M$, $y(t) = \sin \omega_y t$

FIG. 4.3 Indirect method waveforms.

When these waveforms are filtered, the $k_1 y$ component does not appear since the D.C. component of the pulse train responsible for $k_1 y$ is effectively averaged out for each period of the fundamental pulse frequency. This will hold true as long as the pulse frequency is a reasonable factor larger than the frequency of the y signal.

The configuration required to produce these waveforms is more complicated than that used for the direct method. Two choppers are needed as well as a bistable flip-flop. The purpose of the flip-flop is to provide complementary pulses to drive the choppers alternately. Width modulation is introduced by using the pulse width modulator to trigger the bistable flip-flop. The complete system is illustrated in Fig. 4.4 and its waveforms are shown in Fig. 4.5. These waveforms show how the outputs of two D.P. choppers are added to produce the desired output.

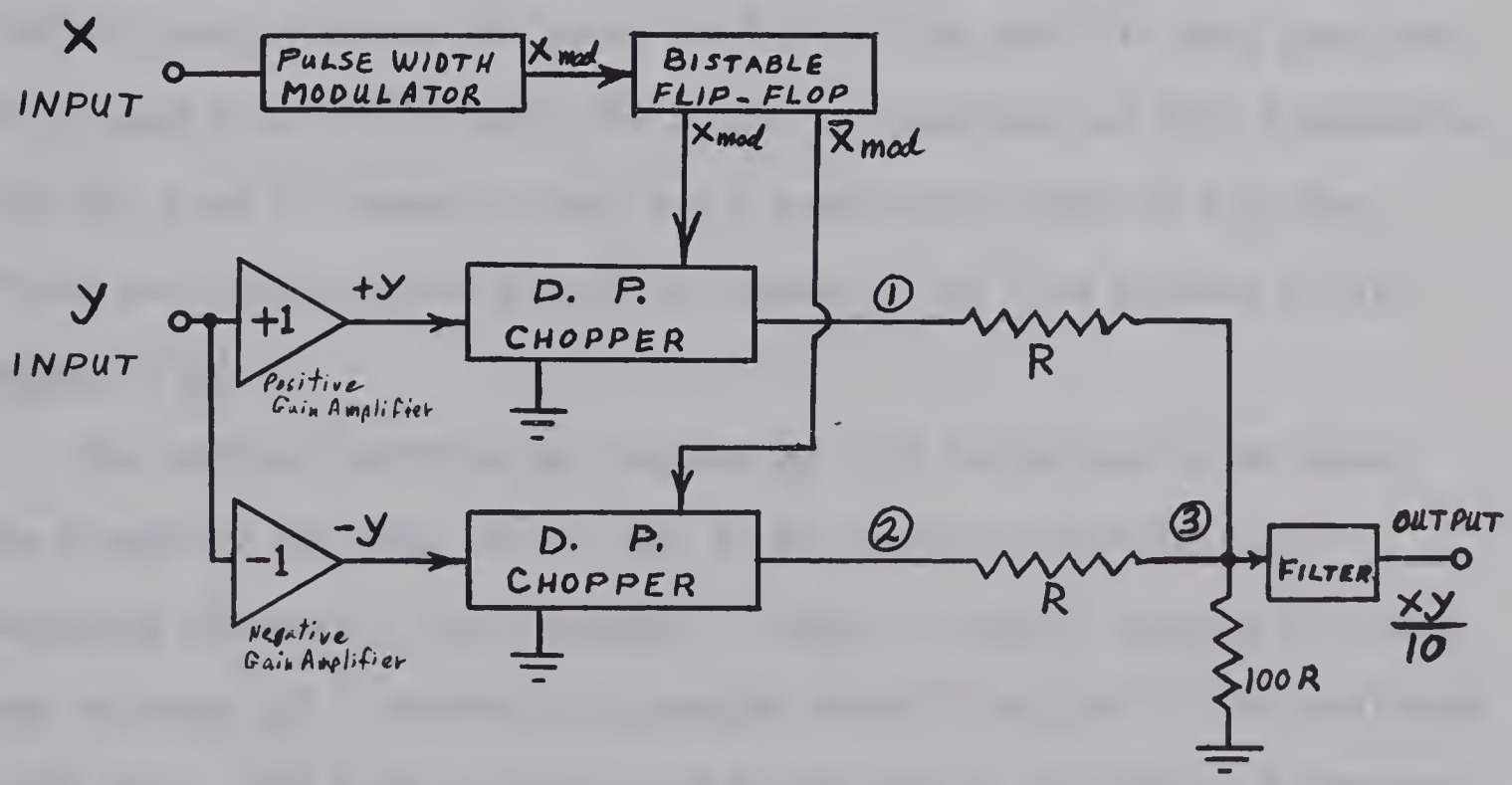


FIG. 4.4 Indirect method use of D.P. choppers.

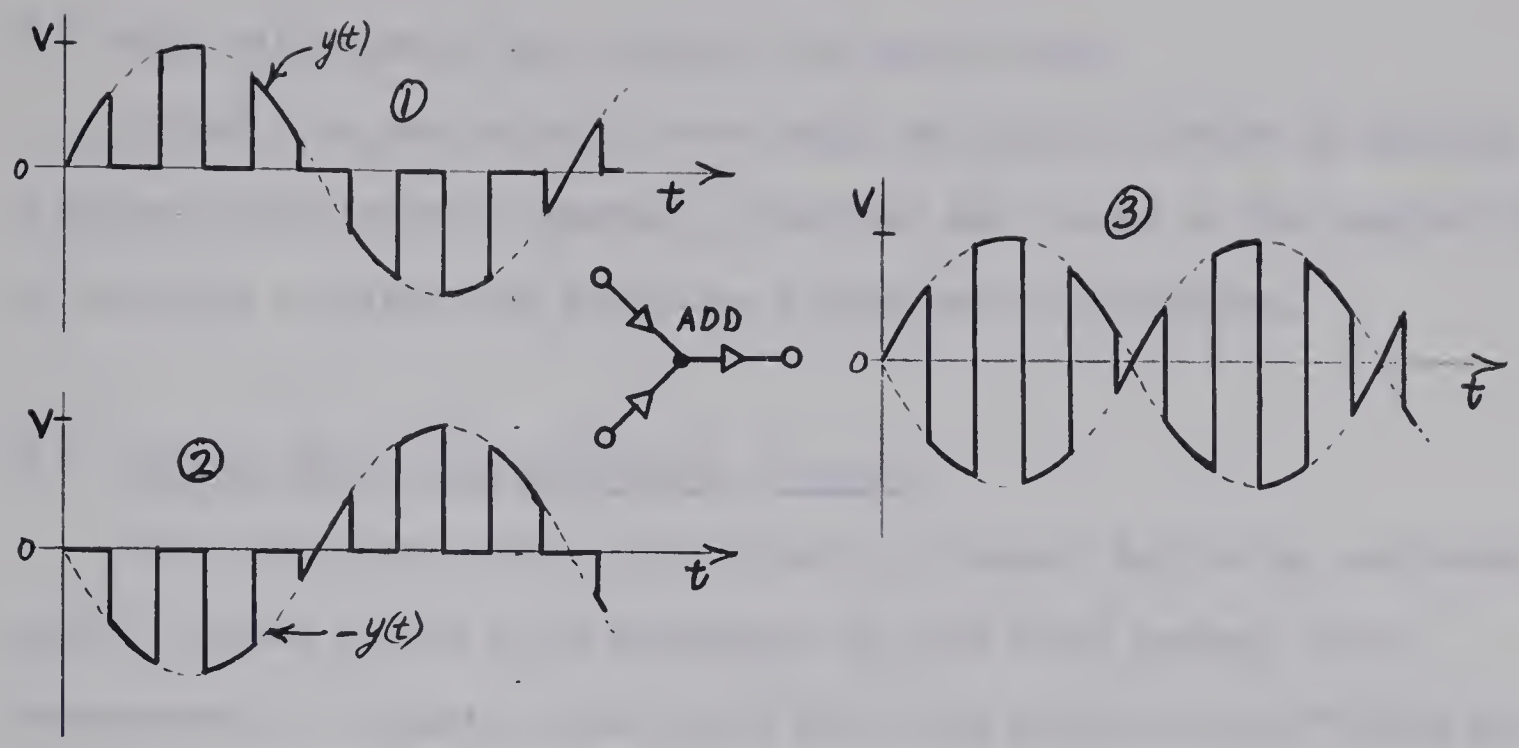


FIG. 4.5 Indirect method waveforms demonstrating formation of output pulse waveform.

Both positive and negative gain input amplifiers were used in the system (in lieu of only one negative gain amplifier) to ensure that the choppers were modulating signals of similar source impedance as well as similar phase shifts. The phase shifts will be small in this case but it is good practice to avoid any chance of imbalance at high frequencies. With the type of summation used and a modulation index of 0.5, the filter section must have a gain of between 4 and 5 to produce a full output of $\frac{xy}{10}$.

The initial performance provided by this system was quite good. The linearity was such that it had to be measured accurately to determine the actual error present. However, careful testing did show that an error of 1 percent to 2 percent overall existed in the amplitude modulation. The failure to produce the desired accuracy was attributed to the unsatisfactory performance of the double polarity chopper used. Attempts to construct a better D.P. chopper were unrewarding. Section

5.5 deals with some of the circuits that were tried.

Rather than persisting in what might be a futile effort to develop a better double polarity chopper, attention was turned to the possibility of devising a system that could use single polarity choppers.

4.2 Systems Using Single Polarity Choppers

Only one system using single polarity choppers had to be considered as this system proved to be acceptable for the final design. The improvement in linearity experienced with this system was sufficient to warrant the increase in complexity needed in the circuitry.

(a) Indirect Method Applied to Single Polarity Choppers

This system is basically similar to that of Fig. 4.3. The differences are mainly in the application of bias voltages to parts of the circuit to allow the use of the single polarity chopper. The configuration of Fig. 4.6 illustrates this use.

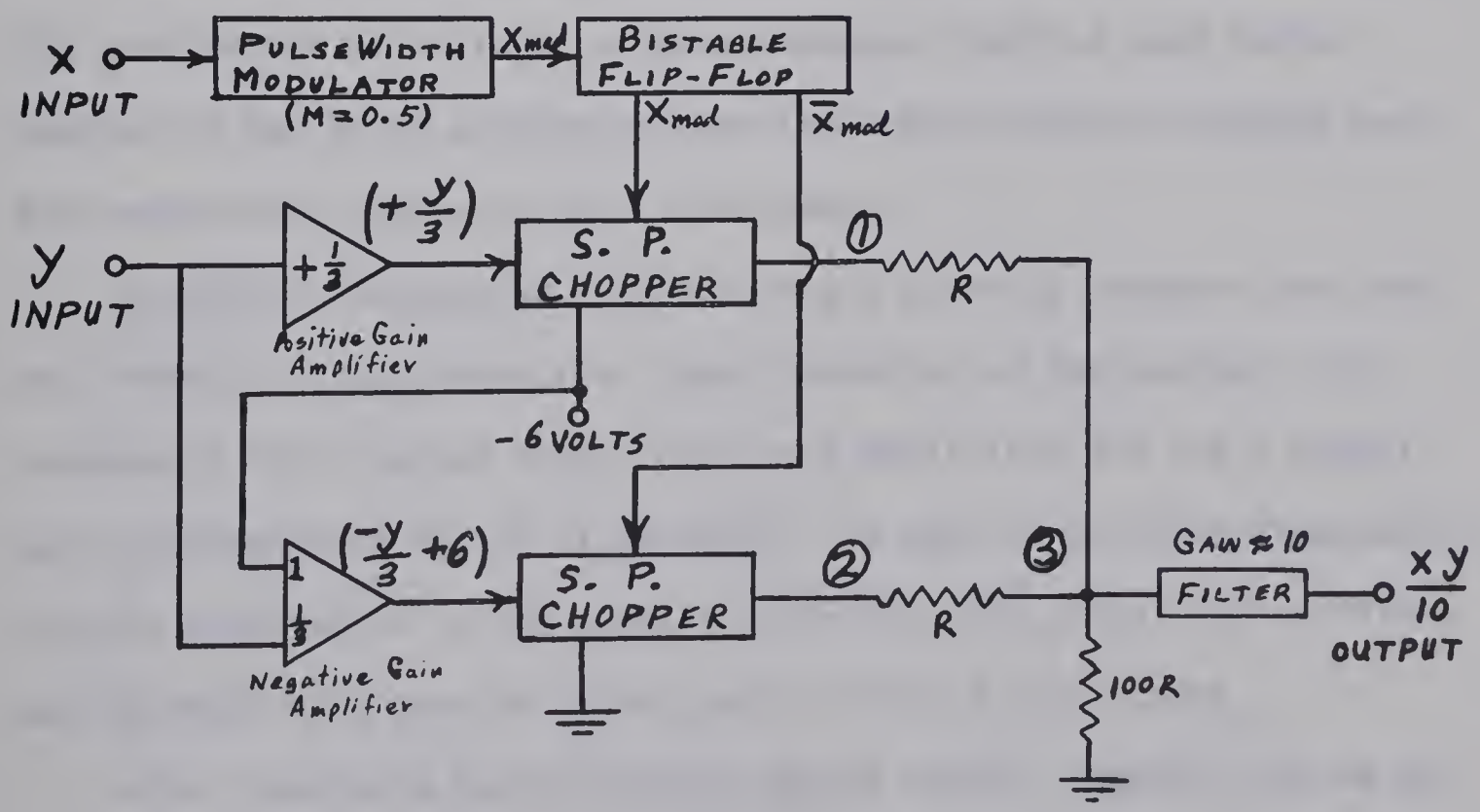


FIG. 4.6 Indirect method use of single polarity choppers.

To understand the operation of the system, the waveforms at various points can be looked at. The construction of the final modulated waveform is illustrated in Fig. 4.7.

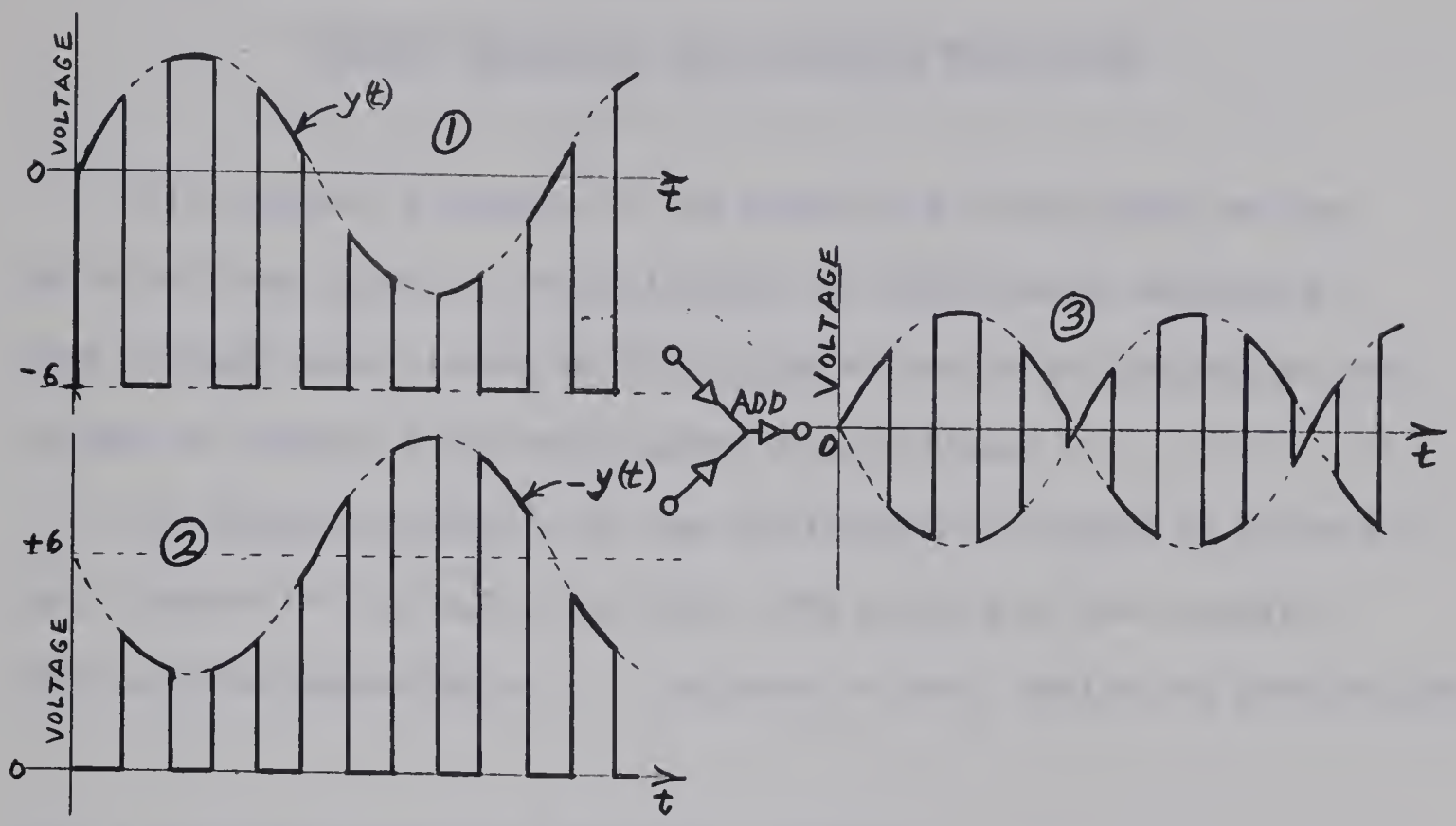


FIG. 4.7 Indirect S.P. method waveforms.

The results produced by this system were by far the best obtained. The development of a single polarity chopper that had much better control of the pulse waveshapes than the double polarity chopper was the determining factor in this improvement.

A problem encountered with the single polarity choppers used was the limited voltage range for linear operation of the devices. To accomodate this limited range, the input amplifiers for the y signal were operated with a gain of about $\frac{1}{3}$. To make up for this attenuation and the attenuation in the summing resistors, the output active filter was operated at a gain of 10 to give a full ±10 volt output.

With a definite multiplication method chosen, emphasis can be put on the detailed design of the building blocks involved.

CHAPTER 5

CIRCUIT DESIGN OF TIME DIVISION MULTIPLIER

This chapter is devoted to the design and construction of the basic building blocks of the multiplier as described in section 4.2. Some of these were already built in simple form to aid testing of the systems of chapter 4 and only needed to be refined.

The completed circuits of the final design are shown at the end of this chapter in Fig.'s 5.32 to 5.38. The details of the circuits are presented approximately in the order of their design and construction.

5.1 Pulse Width Modulator Comparator Section

Pulse width modulation can be implemented most easily by the use of a simple sweep waveform. As shown in Fig. 5.1, the negative going edge that resets the sweep is used to start the pulse. The pulse is ended when the sweep voltage reaches a value that is controlled by the input x. When x = 0, the pulse ends at $V_s = \frac{V_{sm}}{2}$. If x is not zero,

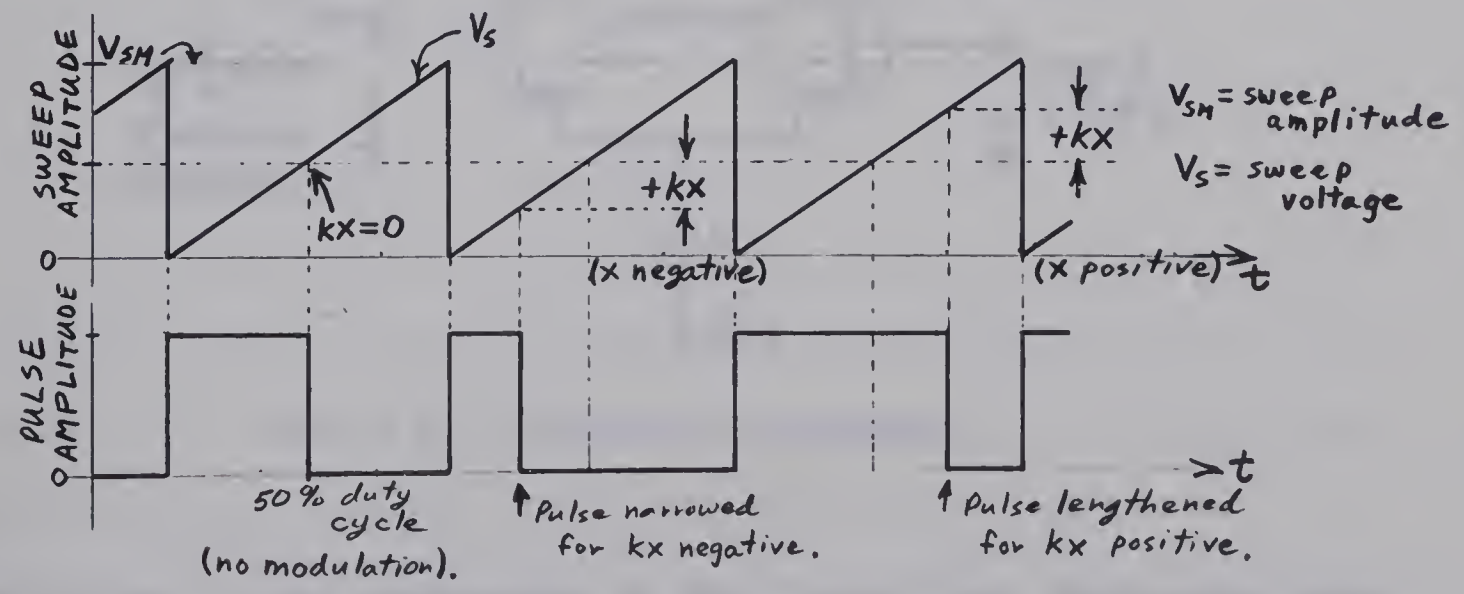


FIG. 5.1 Pulse width modulation waveforms.

then the pulse ends at $V_s = \left(\frac{V_{sm}}{2} + kx \right)$. Thus if x is positive, the pulse width is larger than for x = 0; and if x is negative, the pulse width is smaller. As a result, pulse width modulation is produced.

To obtain the effect shown in the waveforms, a comparator must be used. The comparator "compares" the sweep voltage with the input voltage and switches state of its output only if the sweep voltage becomes larger than the input voltage $(kx + \frac{V_{sm}}{2})$. The comparator also will switch back to its original state when the sweep resets. The necessity of providing the $\frac{V_{sm}}{2}$ bias voltage for the input can be avoided by using a sweep waveform with a zero average voltage.

A few different types of comparators were considered before the final choice was made.

(a) Differential Comparator

This comparator type is logically one of the first that should be considered. It has inherently good temperature drift characteristics and its simplicity is appealing. However, there were some basic

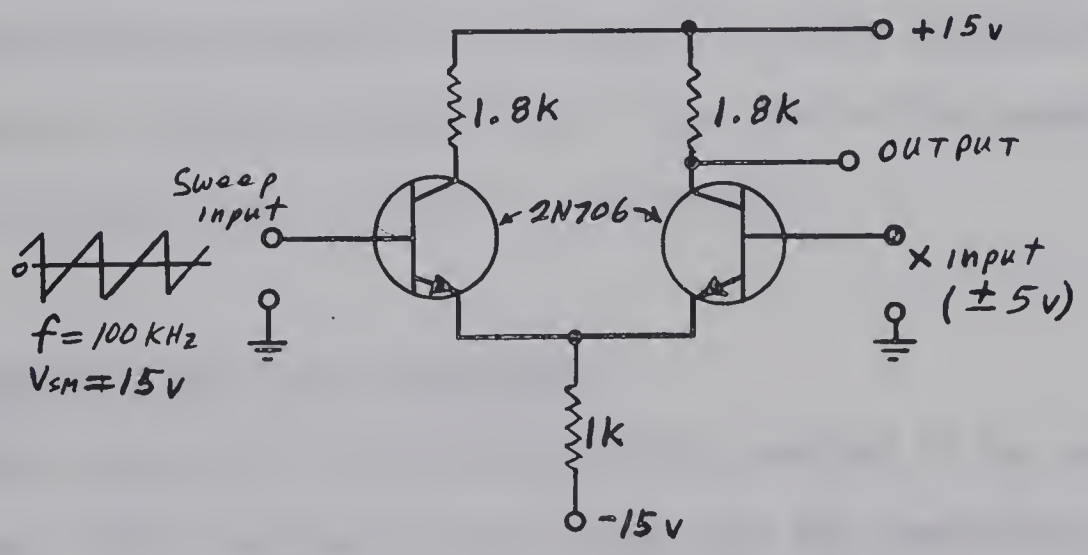


FIG. 5.2 Differential comparator.

limitations to the performance of this circuit that diminished hopes

that it could be made to operate properly in this application. One problem recognized quite early was the need for a very high gain in the comparator in order to obtain fast risetimes. This did not appear possible for the simple two transistor circuit alone. Also, there were indications that the circuit was inherently slow and that an adequate gain would not be enough to give the risetimes desired. Another minor annoyance was an output waveform that varied in amplitude with the input voltage. After trying a two stage comparator (using 4 transistors) and not obtaining promising performance, the circuit was set aside for possible future consideration if no other method proved satisfactory.

(b) Schmitt Trigger

Because of the reputation of this circuit for its speed, it merited some attention. Study of the circuit indicated that introducing the modulation (or "comparison") would cause some difficulties and that temperature drift would be a problem.

Neither of these problems seemed unsolvable, but before any solution could be attempted a new approach to the comparator was discovered. This new approach was in the form of the possible use of a hybrid tunnel diode circuit as a comparator.

(c) Hybrid Tunnel Diode Comparator

This circuit has the characteristics desired in the comparator required. The risetimes are very short and the comparator is very convenient to modulate. To understand the operation of the circuit, it is necessary to know a few facts about tunnel diodes.

(1) Tunnel Diodes

The basic operation of a tunnel diode is indicated in Fig. 5.3.

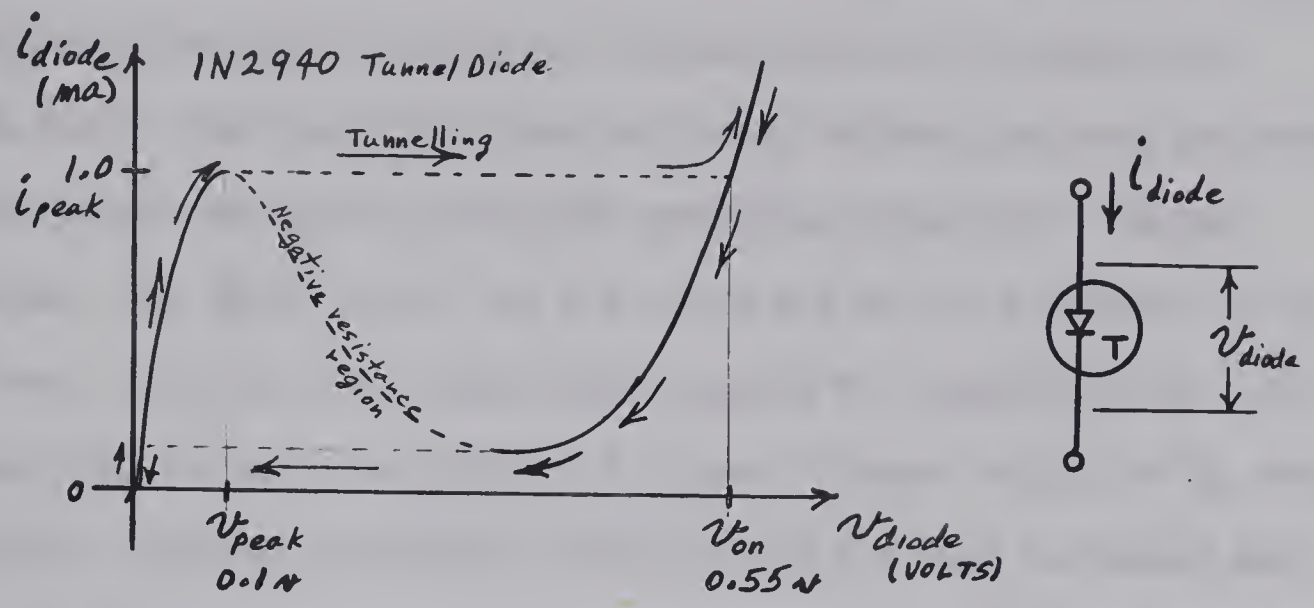


FIG. 5.3 Tunnel diode characteristics.

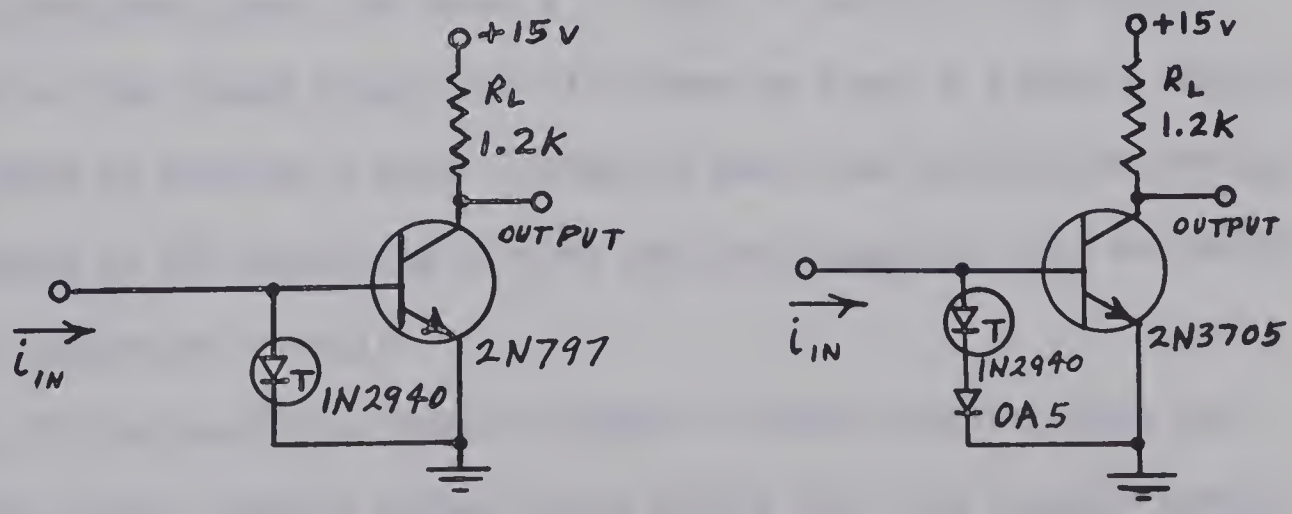
As the current in the diode is increased, initially the voltage across the diode increases only slightly. When a critical value of current is reached, a "tunnelling" of electrons through a potential barrier suddenly occurs. The result is that the voltage across the diode very quickly jumps from about 0.1 volts to about 0.5 volts. From then on, as the current is increased, the voltage increases as it would in a normal diode. The diode will recover to its original state only if the current is reduced to a minimum current called the valley current. Here tunnelling again occurs and the diode is once more ready to repeat the cycle.

(2) Basic Hybrid Tunnel Diode Circuit

The voltage jump produced by the tunnel diode can be used to turn a transistor ON and OFF if the transistor is chosen properly. For a 1N2940 tunnel diode: i_{peak} = 1 ma, v_{peak} = 0.1 volts, and v_{on} (just after the point of triggering) = 0.55 volts. If a transistor is chosen

that is OFF for a base voltage of 0.1 volts and ON for a base voltage between 0.55 volts and about 0.2 volts, then it will be compatible for operation in the hybrid circuit. The basic circuit is shown in Fig. 5.4(a). The transistor that was found to have the best performance in the hybrid circuit was the 2N797 germanium transistor. Being germanium, the 2N797 is OFF for 0.1 volts and ON for 0.3 volts or more, and thusly satisfies the stated requirements for compatibility. The optimum load resistor was about 1.2 K ohms. Larger values of R_L result in longer risetimes and smaller values cause too much overshoot and ringing. Risetimes of about 0.07 μsec. with little or no overshoot can be obtained with R_L = 1.2 K ohms.

If it is desirable to use a silicon transistor in the hybrid circuit then a germanium diode must be used in series with the tunnel diode to provide sufficient voltage to turn the transistor ON (about 0.65 volts is needed). Fortunately, the Ge diode voltage is not so large as to turn the transistor ON when the tunnel diode is OFF. Fig. 5.4(b) shows the OA5 Ge diode being used with the 2N3705 transistor for this purpose. Characteristic curves for these hybrid circuits can be found in references (10) and (11).



(a) Germanium transistor. (b) Silicon transistor.

FIG. 5.4 Basic hybrid tunnel diode circuits.

(3) Application of the Basic Hybrid Circuit in a Comparator

The basic hybrid circuit is a current controlled circuit but the inputs available are voltage inputs, thus some modifications must be made. The circuit of Fig. 5.5 has the changes needed to make it a practical hybrid comparator circuit complete with modulation input.

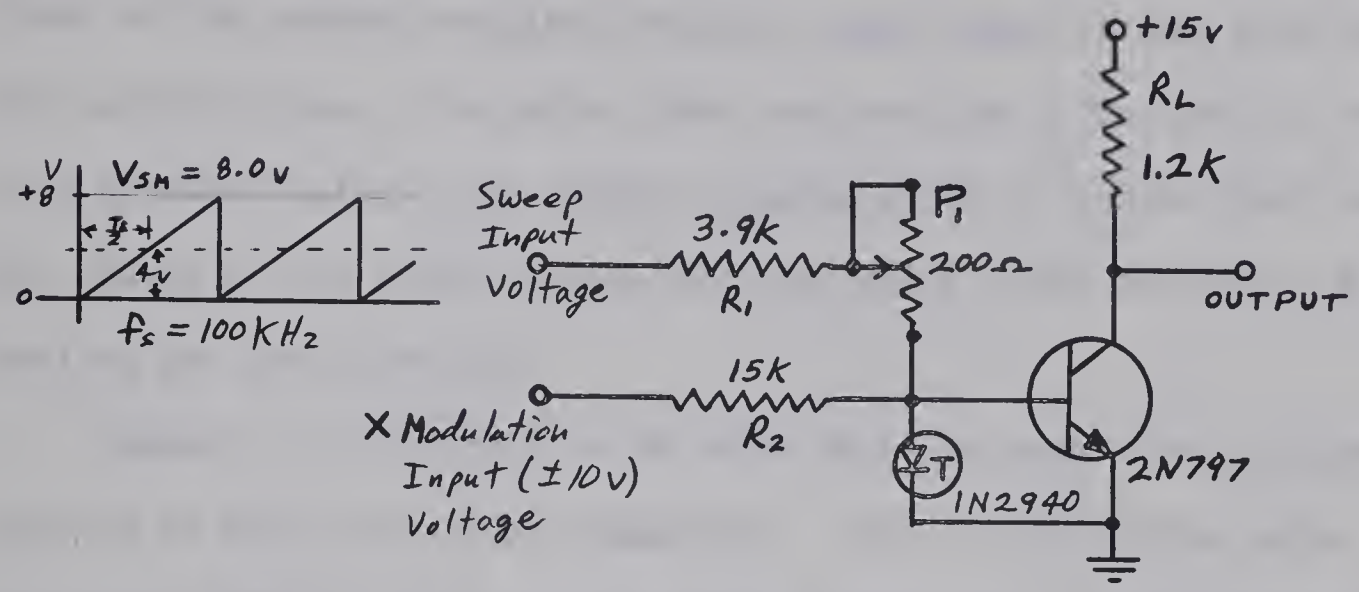
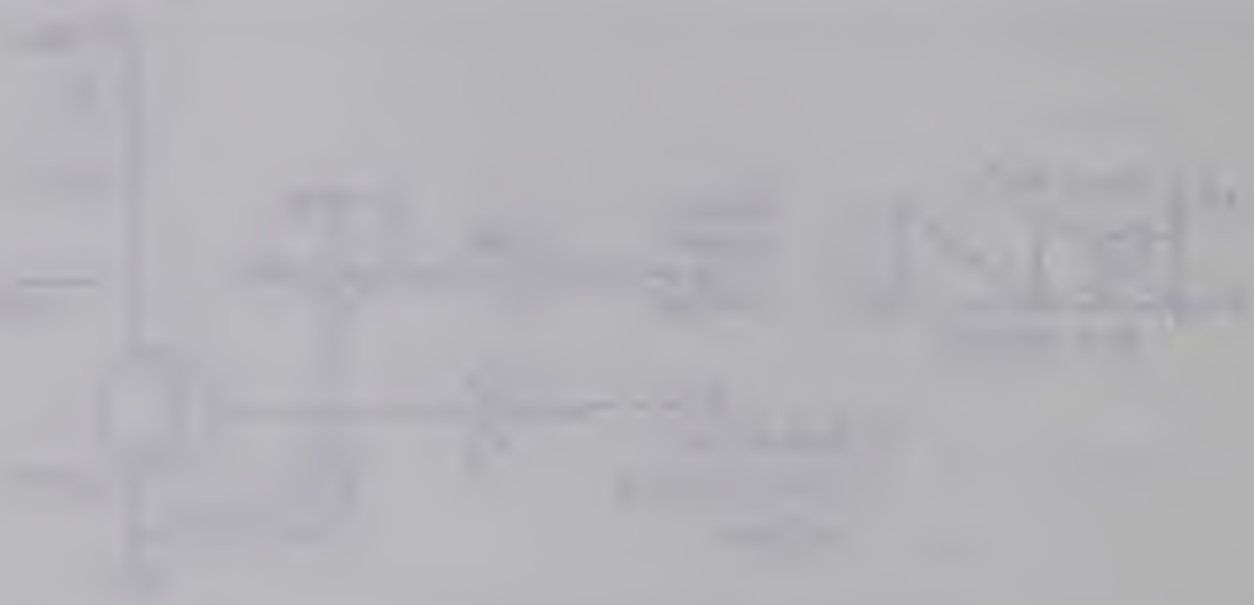


FIG. 5.5 Initial hybrid comparator circuit.

The operation of the circuit is quite straight forward. The comparator is initially adjusted to give an output pulse of 50 percent duty cycle for a zero modulation input voltage. This is done by varying potentiometer P_1 such that the triggering current of 1 ma will pass through the tunnel diode when the sweep voltage reaches one half of its maximum amplitude (ie. when $V_s = \frac{Vsm}{2} = 4$ volts). The total resistance of the sweep input path will then be about 4 K ohms. Notice that the need to provide a bias voltage to the input modulation voltage (as mentioned at the beginning of this section; page 28) does not exist with this comparator circuit.

Now, if the modulation input voltage is made negative, then the sweep voltage will reach a higher value before the 1 ma trigger current will flow in the tunnel diode. This occurs because current is drained



away from the tunnel diode input by the modulation input so a larger total current must be supplied by the sweep input before 1 ma will flow in the tunnel diode. This causes the triggering to occur later in the sweep period and thus a wider pulse is produced. For a positive modulation input voltage, extra current will be supplied to the tunnel diode so the current required from the sweep input is less than for the quiescent case. The pulse then ends earlier in the period, resulting in a narrower pulse. The change in pulse width is proportional to the change of the input voltage thus the pulse width modulation effect desired has been achieved.

However, a difficulty arises when positive modulation voltages are applied to the constructed comparator. This is due to the large hysteresis effect in the tunnel diode triggering. In order for the tunnel diode to be reset at the end of a sweep, the current in the diode must be reduced to almost zero. If the modulation voltage is zero or negative the tunnel diode current will become zero or negative when the sweep voltage resets and the diode will be reset properly. But if a positive voltage is applied to the modulation input, current will continue to flow positively in the tunnel diode even after the sweep voltage resets. If the current is large enough, the diode will fail to reset and the output pulses will cease.

There is an easy solution to this problem. This calls for the provision of a special reset pulse.

(4) Reset Pulse

To ensure that the tunnel diode resets for all modulation conditions, a short negative current pulse of about 2 ma is generated and fed into the tunnel diode at the same time the voltage sweep resets.

The simplest way to form this pulse is to use the negative going reset edge of the sweep voltage to generate a negative current spike. A simple series resistor-capacitor network provides a suitable pulse. The circuit values shown in Fig. 5.6 were obtained with a quick trial and error procedure.

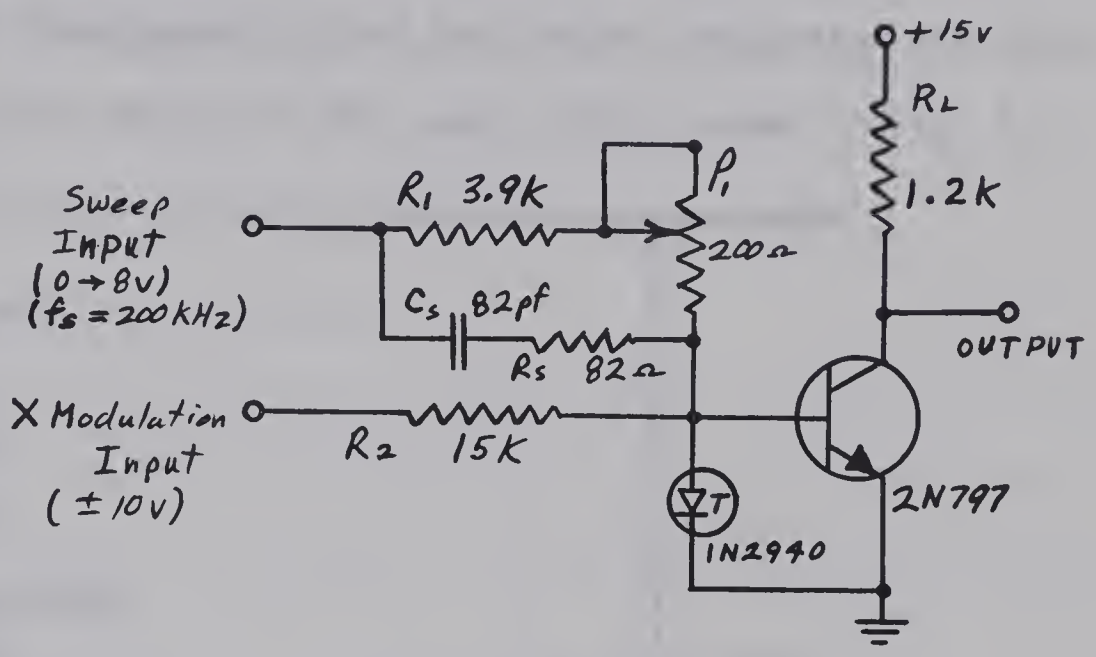


FIG. 5.6 Final hybrid comparator circuit.

The current spike generated by the new network was of sufficient amplitude (3 ma) to guarantee reliable operation regardless of the modulation voltage and yet was short enough (0.6 μsec.) not to interfere with the depth of modulation desired.

With the comparator developed sufficiently, attention was turned toward developing a good linear sweep waveform.

5.2 Sweep Generator Section of Pulse Width Modulator

Various types of sweep circuits were studied before a suitable circuit was developed.

The first sweep circuit built [7] was used temporarily for testing until much of the other multiplier circuitry was developed. It had

reasonable speed but lacked sufficient linearity.

To obtain the linearity required a Miller sweep circuit was built as well as an integration circuit using an operational amplifier. Although the sweep section of the waveform appeared good in these circuits, the delay in resetting the sweep was too long to be tolerable.

However, the development of the fast hybrid comparator discussed previously led to the design of the sweep circuit shown in Fig. 5.7.

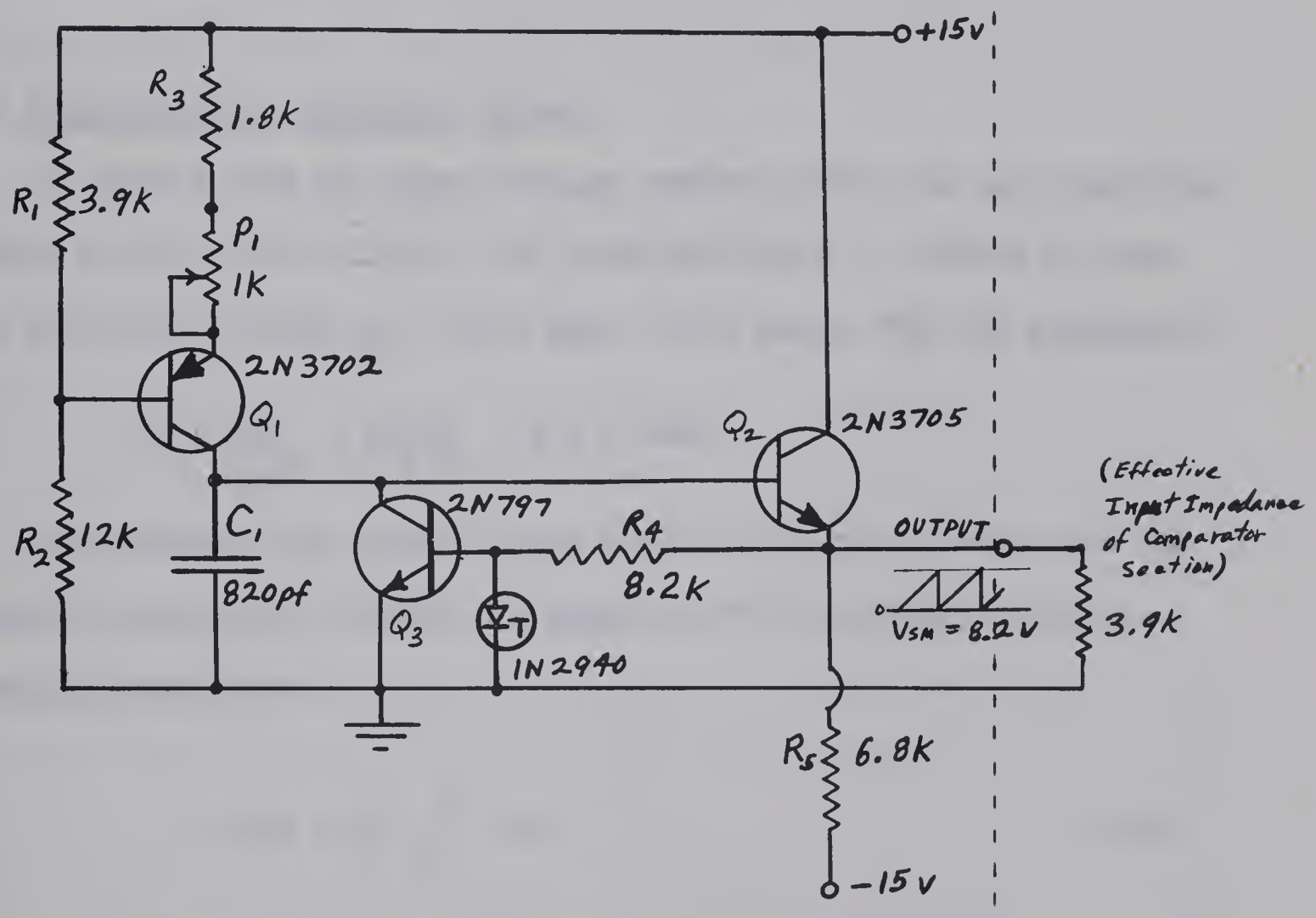


FIG. 5.7 Basic sweep circuit.

Basically, the circuit is just a simple constant current generator charging a capacitor. The result is a capacitor voltage that is a linear function of time. An emitter follower is used as a buffer amplifier to avoid loading the capacitor with a low impedance. Any impedance that does appear across the capacitor will result in

nonlinear "drooping" of the sweep. When the output of emitter follower Q_2 reaches the desired sweep amplitude V_{sm} = 8.2 volts, the comparator is triggered and transistor Q_3 rapidly shorts the capacitor C_1 to ground. When the output voltage reaches zero the comparator resets, turning Q_3 OFF, and the capacitor is allowed to start charging once more. The cycle will repeat regularly and produce the sawtooth waveform desired.

(a) Computation of Component Values

To ensure that the sweep voltage remains within the safe operating limits of the current source, the sweep amplitude is limited to about 8.2 volts by choosing R_4 = 8.2 K ohms. This comes from the expression

$$R_4 = \frac{V_{sm}}{i_{peak}} = \frac{8.2 \text{ v}}{1.0 \text{ ma}} = 8.2 \text{ K ohms.}$$

To determine the values of the constant charging current and the capacitor required, consider the equation for the voltage across a charging capacitor:

$$v(t) = \frac{1}{C} \int_0^t i \, d\tau \, . \qquad (5\text{-}1)$$

Since i is a constant current equal to I_c then

$$v(t) = \frac{1}{C} I_c \, t$$

and

$$I_c = \frac{v(t)}{t} \, C \, . \qquad (5\text{-}2)$$

For a repetition rate of 200 KHz (which was the final f_s chosen) the corresponding period is $T_s = \frac{1}{f_s} = 5$ μsec. Allowing for 0.1 μsec reset time gives 4.9 μsec of sweep time. Thus the voltage gradient of the sweep is

$$G_v = \frac{v(t)}{t} = \frac{8.2 \text{ v}}{4.9 \text{ μsec}} = 16.73 \times 10^5 \text{ v/sec} .$$

To avoid the possibility of stray capacitance affecting the sweep rate, a value of 820 pf was chosen for C_1. Substitute G_v and C_1 into eq. (5-2) to get

$$I_c = G_v C = (16.73 \times 10^5)(820 \times 10^{-12}) = 1.37 \text{ ma} .$$

This was considered a reasonable value of current and was accepted. The current produced by the current generator depends on the value of R_3 and the voltage across it. To minimize the effect that variation of the base voltage of Q_1 with temperature will have on I_c, the voltage across R_3 is made as large as is practical. If V_{R_3} is chosen to be 3.0 volts, a safety margin of 3.8 volts is left to ensure that Q_1 keeps in its linear operating region and well out of saturation. The voltage across R_1 will then be $V_{R_1} = 3.0 \text{ v} + 0.6 \text{ v} = 3.6$ volts. The resistor $R_3 = 3.0 \text{ v} / 1.37 \text{ ma} = 2.2$ K ohms. To allow for adjustment, a 1.8 K ohm resistor and a 1 K ohm potentiometer can be used in series. With a value of 2.2 K ohms in the emitter path of Q_1, a total resistance of about 15 K ohms is suitable for its base biasing network. Consider the equation

$$V_{R_1} = (15.0 \text{ v}) \times \left(\frac{R_1}{R_1 + R_2}\right) = 3.6 \text{ volts} .$$

Then

$$R_1 = R_T \frac{3.6\ v}{15.0\ v} = (15 \times 10^3)(\frac{3.6\ v}{15.0\ v}) = 3.6\ K\ ohms\ .$$

The nearest standard value of 3.9 K ohms is chosen for R_1. The resistor R_2 is then computed as

$$R_2 = \frac{11.4}{3.6} R_1 = (3.17)\ (3.9 \times 10^3) = 12.3\ K\ ohms\ .$$

The nearest standard value of 12 K ohms is chosen for R_2. There is sufficient adjustment in the potentiometer P_1 to compensate for the error in frequency that may occur due to the alteration of R_2 and the tolerances of the components involved.

The emitter follower resistor is still to be chosen. Since the emitter follower does not have to drive loads that terminate at a higher voltage than the emitter voltage, the choice of R_5 is not critical. It should be small enough to keep Q_2 from getting close to cutoff as h_{ib} increases rapidly in this region. Since changes in h_{ib} affect the gain of the emitter follower it is wise to keep them as small as is practical. To preserve the input impedance, R_5 cannot be made too small. A value of 6.8 K ohms was chosen as it gives emitter currents from 2 ma to 9 ma which is a reasonable current variation. The input impedance will still be at least 200 K ohms.

(b) Improvement of Linearity

The circuit design at this point is such that the effect of the emitter follower nonlinearity, the current source nonlinearity, and the loading of the capacitor C_1 by the emitter follower input impedance, are not negligible. Tests showed that a total error of between

1 percent and 2 percent existed due to these causes. Calculations indicate that the total error introduced by the emitter follower is about 0.4 percent thus the major part of the error is essentially due to the loading of the capacitor by the emitter follower input impedance, the OFF impedance of the comparator output, and the current source output impedance. Attempts were made to raise the input impedance of the buffer amplifier (ie. emitter follower originally) by the use of circuits such as complementary compound connected transistors in an emitter follower configuration and the use of a field effect transistor in a unipolar-bipolar source follower configuration. However, raising the impedance level at the capacitor had the undesirable effect that noise pickup (RF noise, TV signals, etc.) caused the reset edge of the sweep to jitter.

Before attempting to solve this problem by employing shielding to avoid pickup, consideration was given to another possible solution of the linearity problem itself. The linearity tests showed that the deviation from linearity was approximately parabolic when plotted on a graph as shown in Fig. 5.8.

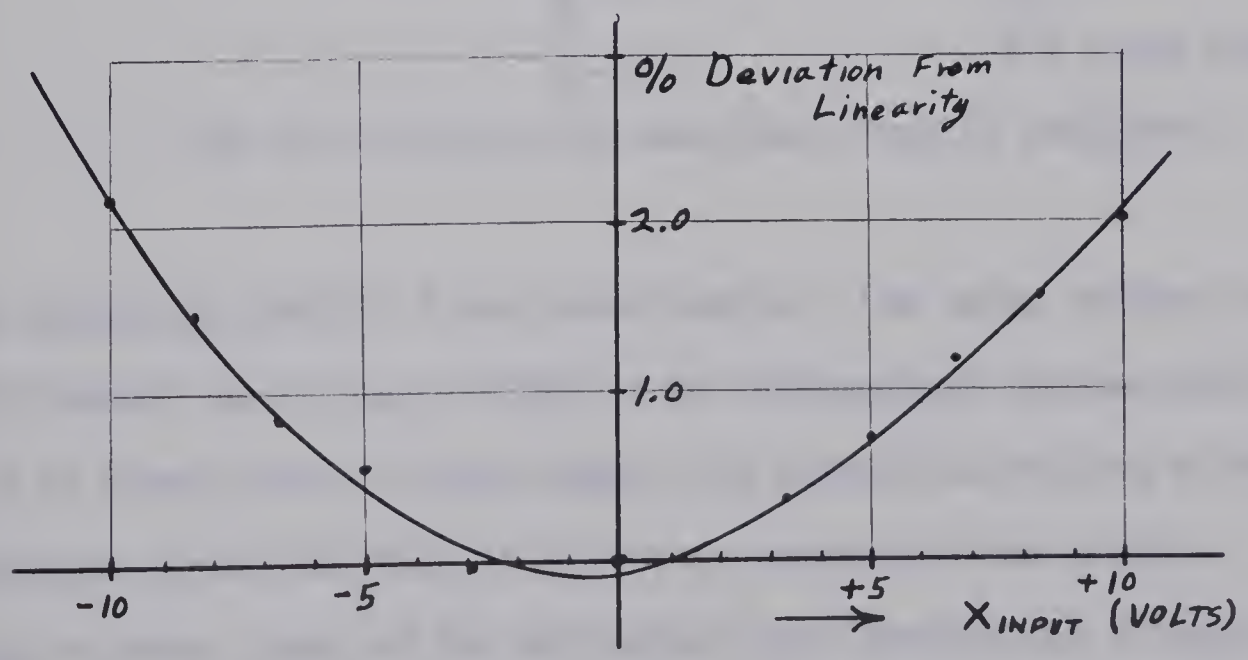


FIG. 5.8 Width modulator error.

This smooth error graph is not unexpected since most of the error is due to the "drooping" of the sweep as mentioned previously. The logical solution to this type of error is to use a type of feedback that increases the charging current as the sweep voltage increases and thus replace the current lost through the loading impedances. The additions necessary to employ the feedback are shown in the circuit of Fig. 5.9 (which shows the almost completed width modulator).

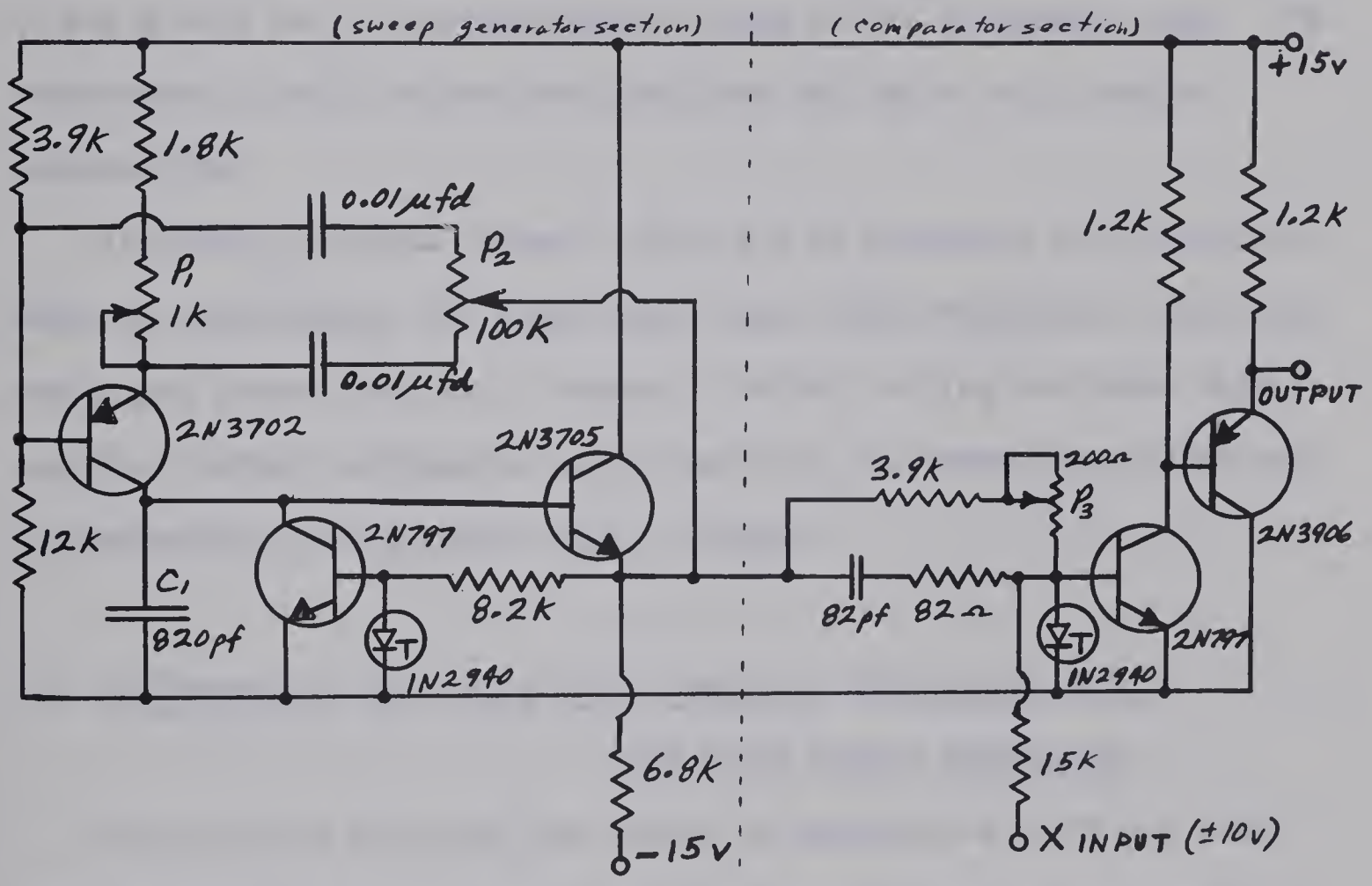


FIG. 5.9 Pulse width modulator (nearly complete).

By adjusting the 100 K ohm potentiometer, the sweep voltage can be made to "droop" up or down. There is an intermediate setting which results in a very nearly linear sweep. An attractive feature of this compensation circuit is that it will also compensate for errors produced in other parts of the multiplier that involve the x signal path, as long as they are similar in nature to that shown in Fig. 5.8.

The merits of this compensation were evident when the complete multiplier was tested. A 1 KHz signal (with an amplitude of ±10 volts) was fed into the x input. With no compensation, the second harmonic frequency component (which is the main distortion component) was measured at the output as 57 db below the fundamental frequency. When the compensation was connected and adjusted, the second harmonic was measured as 67 db below the fundamental. This figure was so low that it was almost out of the measurement range of the instrument used. The improvement is self evident and justifies the use of this type of compensation.

The width modulator shown in Fig. 5.9 is developed sufficiently to meet the requirements for sweep reset time, width modulation linearity, and output pulse risetimes. However, further testing indicated that it requires further refinements with respect to its temperature drift and its dependence on the power supply voltages.

5.3 Refinement of the Pulse Width Modulator Temperature Drift and Power Supply Dependence

This section discusses the causes of temperature drift and power supply dependence and then describes the methods used to improve them.

(a) Temperature Drift

Temperature drift in the width modulator results from several causes. This drift (in the order of 0.1 percent/^{o}F to 0.2 percent/^{o}F) is not tolerable since it appears as an effective voltage offset in the x input voltage. When this drift appears at the output it does so in the form of a voltage multiplied by the y input signal in the same way

as the x input signal is multiplied. The result is a residual y signal voltage that degrades the accuracy of the multiplier. For this reason the drift must be compensated for in the width modulator itself rather than another part of the multiplier (such as the output amplifier). This is the best procedure to follow in any case.

Conducting a series of temperature tests on the circuit of Fig. 5.9 reveals that the major portion of the drift occurs in the comparator due to the drift of i_{peak} of the tunnel diode. This current parameter varies quickly with changes in temperature and can drift as much as 0.1 percent/^{o}F. This was more than expected as at least one reference[6] stated that i_{peak} was reasonably stable (about 5 percent change for a temperature change of 150^{o}C). However, the tunnel diodes available did drift and had to be compensated for.

Drift also results from the hybrid comparator in the sweep circuit. Drift in the comparator results in a change of the sweep amplitude. For example, if the amplitude increases the point at which the output pulse ends occurs sooner in the period than previously. This represents an equivalent change in the x input. This effect is illustrated in Fig. 5.10.

Other sources of drift are due to the emitter follower drift in the sweep circuit (about 0.04 percent/^{o}F) and frequency drift (caused by current source drift). Frequency drift would not cause the modulator to drift if it were not for the finite value of sweep reset time. As the length of the period changes the ratio of the sweep time to reset time changes and thus the pulse width changes for the same x input voltage. In this case, the effect is small because the current source does not drift a great deal.

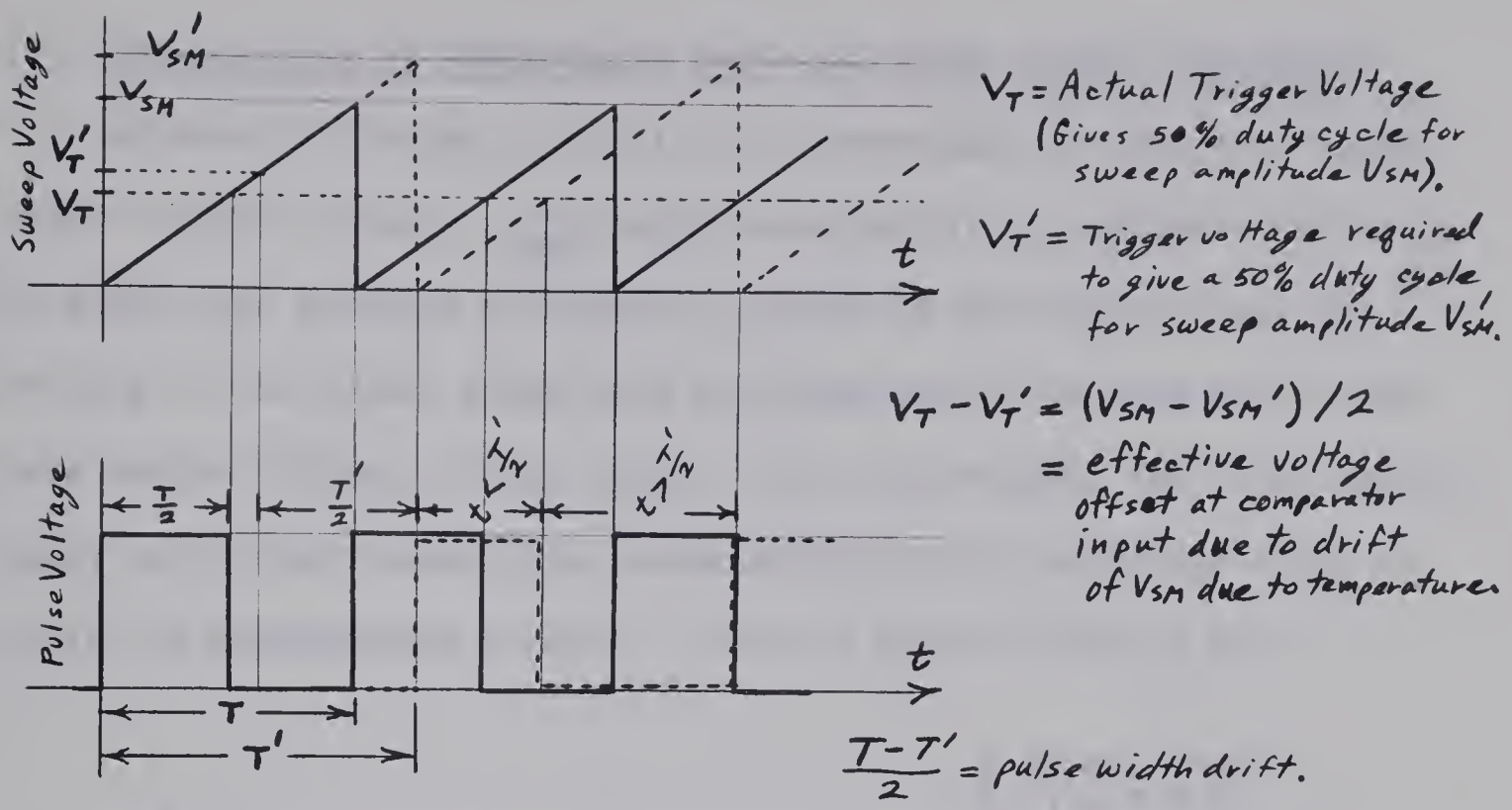


FIG. 5.10 Sweep amplitude drift effect.

(b) Power Supply Dependence

Frequency variations are caused by power supply variations as well as temperature variations. This occurs because the current source varies directly with the supply voltage. The frequency changes that result cause pulse width changes as previously mentioned in section 5.3(a). However, these changes can be much larger than before because the allowance for power supply changes will cause a larger current source change than occurs for the allowable temperature change.

Other causes of power supply dependence result from the implementation of methods of temperature compensation. For this reason, the methods used to solve the two problems are discussed together.

(c) Compensation of Temperature Drift and Power Supply Dependence

Attempts to design a circuit that minimizes the effect of tunnel diode trigger current, i_{peak}, were unsuccessful as complexities had to be added that defeated the overall purpose of the circuit (eg. the driving of the tunnel diode with a voltage source to make use of the more stable trigger voltage v_{peak}). For this reason, the final design makes use of the temperature characteristics of a germanium diode to apply the compensation directly. This is shown in Fig. 5.11.

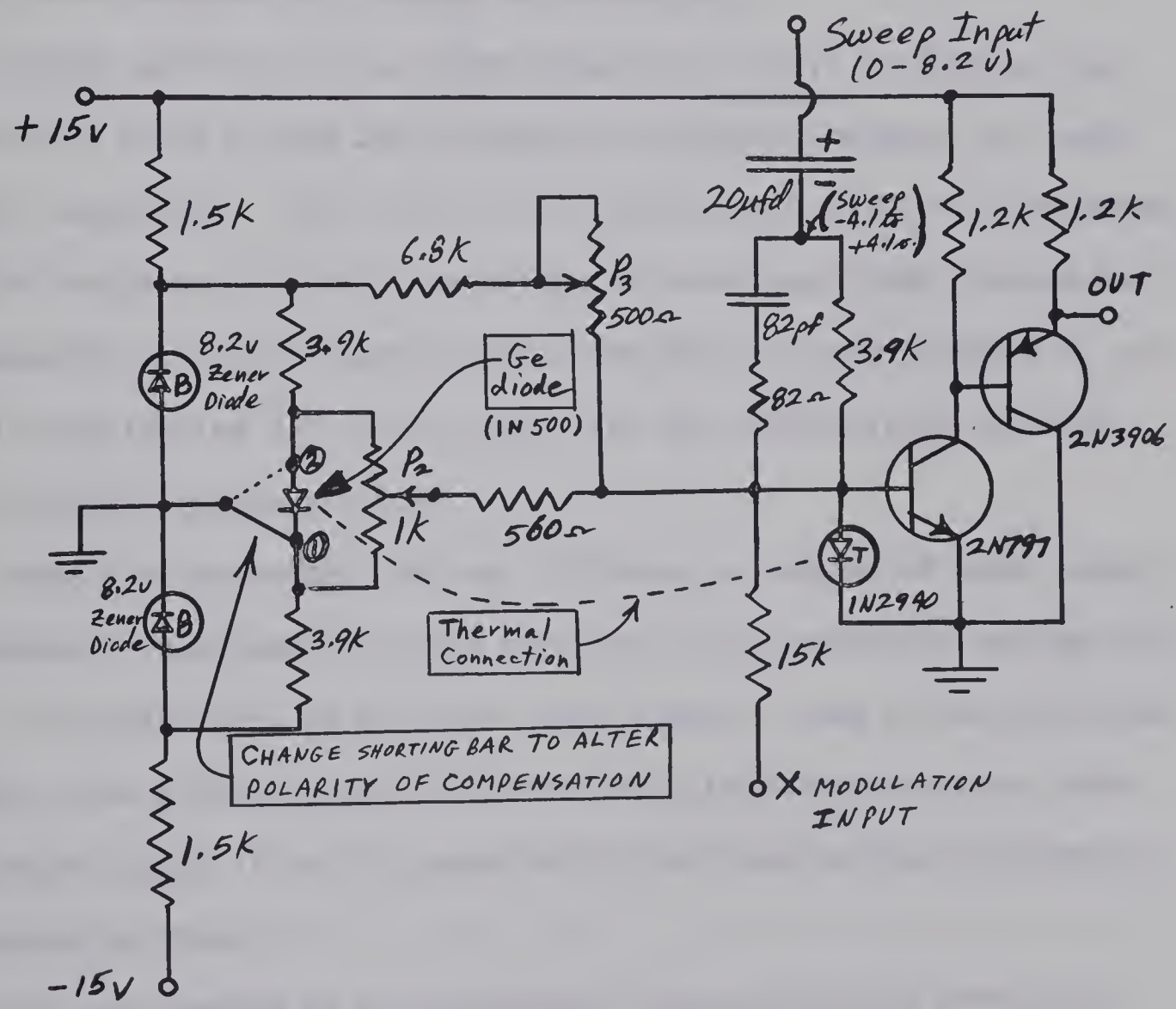


FIG. 5.11 Comparator temperature compensation.

By varying potentiometer P_2, the amount of compensation provided by the germanium diode can be controlled. By performing a series of

temperature tests, P_2 can be adjusted so that the tunnel diode drift can be cancelled quite well over a reasonable temperature range (see temperature test #4). The compensating network is arranged so that the polarity of the compensation may be changed if necessary. Once the polarity is chosen, the unnecessary components may be removed. Fortunately, the germanium diode used for compensation reacts quite quickly to temperature changes. Being nearly as fast as the tunnel diode, the compensation is relatively swift and the voltage excursions due to rapid temperature changes are minimized.

Another addition to the width modulator circuit to improve the temperature drift is the use of capacitor coupling between the sweep and the comparator. This gives a self zeroing capability to the sweep waveform and thus minimizes the effect of sweep amplitude changes due to temperature. A 6.8 K ohm resistor and 500 ohm potentiometer P_3 are used to provide the D.C. bias current for the tunnel diode that the sweep itself formerly provided.

These two improvement methods introduce a problem of power supply dependence if the supply is used directly as the reference voltage for them. To avoid this, an 8.2 volt zener diode is used as the reference voltage. The slight temperature drift in pulse width that the zener diode might cause is easily cancelled by the compensation provided by the germanium diode.

The last problem to be considered is current source drift and power supply dependence. The drift expected from the current source is only about 0.075 percent/^{o}C but compensation is not too difficult so it is worthwile. The circuit shown in Fig. 5.12 provides both reasonable temperature drift compensation and power supply isolation.

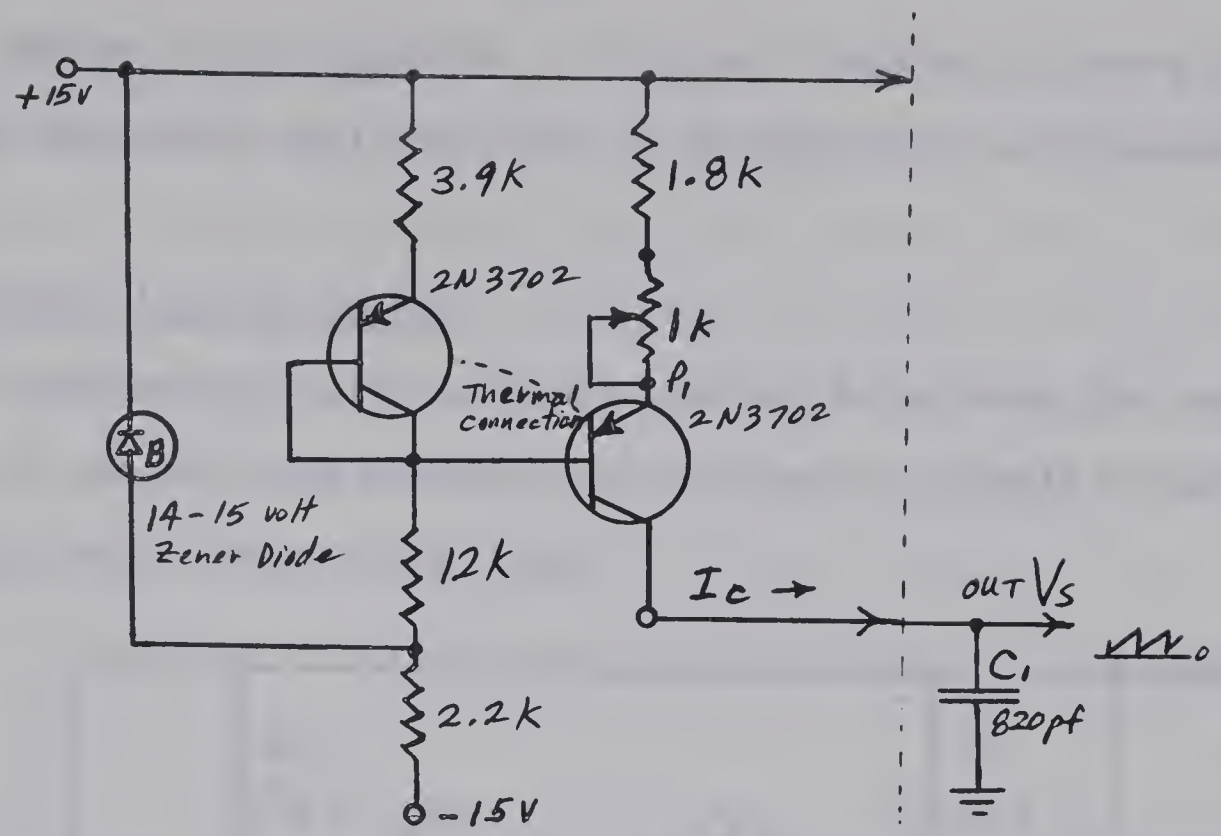


FIG. 5.12 Compensated current source.

The drift for this circuit is only 0.01 percent/^{o}C (see temperature test #12), and power supply variations have little effect.

(d) Input Buffer Amplifier

Only one more circuit needs to be dealt with before the width modulator design is complete. This circuit is an input amplifier for the x input signal. The need for this arises from the fact that the voltage across the tunnel diode is a small but finite value at the trigger point. Thus, when the x input resistor is moved from the floating state to the grounded state, a current change will occur in the resistor and thus cause an undesirable change in pulse width. By using an input amplifier, the amplifier output can be adjusted so that there is no change whether the amplifier input is floating or grounded. This will make the multiplier independent of the x input source impedance, which is an important feature to have.

The design of this amplifier is left until section 5.7 where all the input operational amplifiers used in the multiplier are discussed.

5.4 Bistable Flip-Flop Design

The complementary pulse waveforms required for driving the chopping circuits of the amplitude modulator are provided by a simple bistable flip-flop circuit shown in Fig. 5.13.

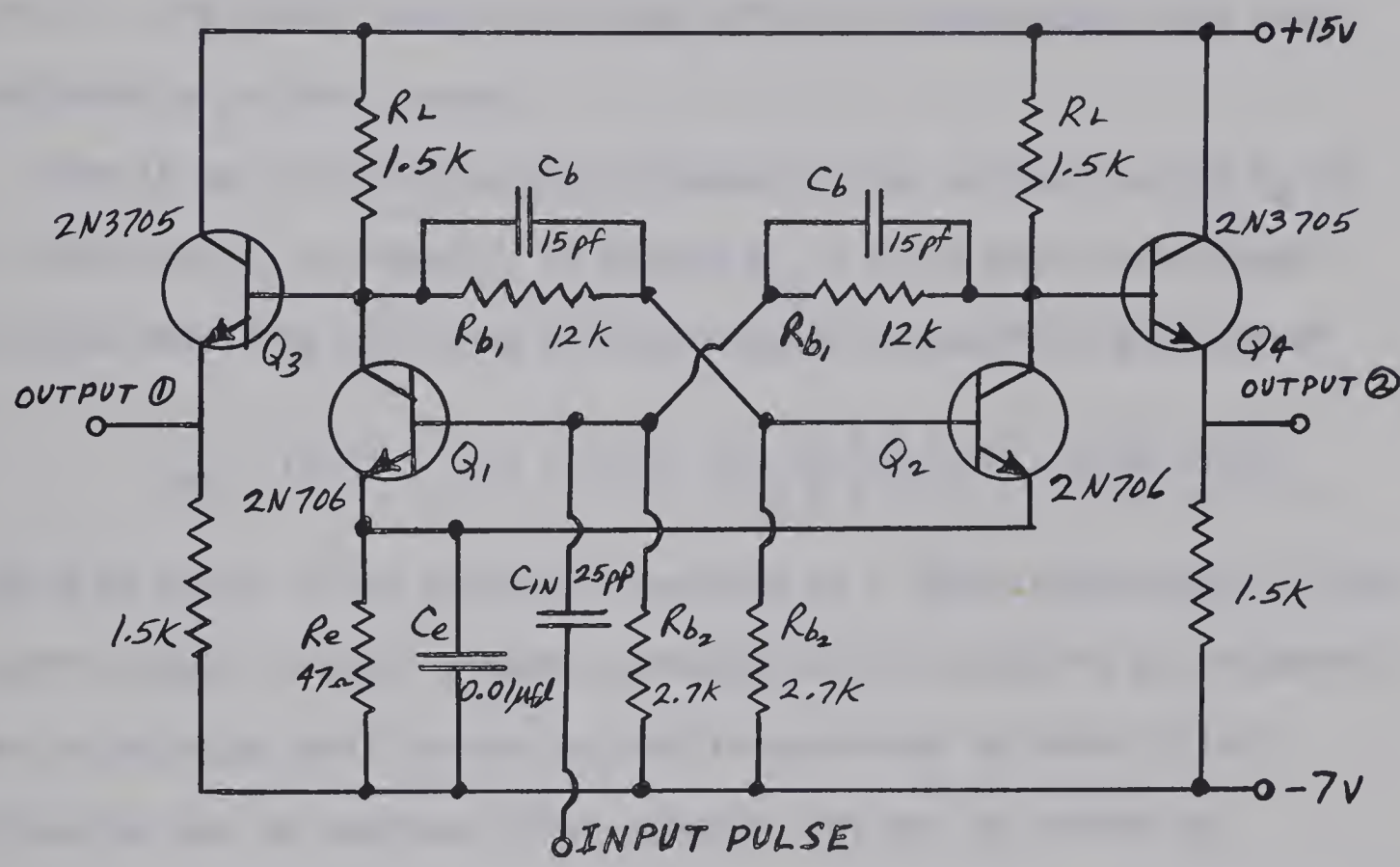


FIG. 5.13 Bistable flip-flop.

The circuit is simple because only a simple triggering method is needed to produce the effect desired. The flip-flop has to change states for each positive and negative going edge of the input pulse train from the width modulator. Only a small capacitor connecting the input pulses to the base of one of the flip-flop transistors (Q_1 or Q_2) is needed to accomplish this.

(a) Choice of Resistor Values

Experimentation indicated that a value of R_L = 1.5 K ohms was suitable for the 2N706 transistors used. The risetimes were as short as possible without too much overshoot with this choice. By choosing R_{b_1} = 12 K ohms a current of 1.6 ma is provided to ensure saturation of Q_1 or Q_2 when the collector current of 15 ma is flowing. Any transistor with a gain of 20 or more will operate properly in this circuit. The 2N706 transistors have sufficient speed even when saturated heavily in this circuit.

The 15 ma collector current produces a bias voltage across R_e of 0.7 volts for R_e = 47 ohms. By making R_{b_2} = 2.7 K ohms the voltage division resulting will give a reverse bias to the OFF transistor of

$$V_{eb} = (0.7) - (0.7 + 0.07)\left(\frac{2.7\ K}{2.7\ K + 12\ K}\right) = 0.56 \text{ volts.}$$

(The 0.07 volts is the saturation voltage of a 2N706 transistor.) This cutoff voltage is small enough to enable the flip-flop to be triggered with relatively small pulses and yet large enough to avoid false triggering due to spurious noise signals that may be picked up.

The emitter follower resistor is chosen as 1.5 K ohms to give a reasonably low output impedance.

(b) Choice of Capacitor Values

With the pulse amplitude available from the width modulator, a value of C_{in} = 27 pf is all that is needed for reliable triggering of the flip-flop. The value of C_{in} is made as small as possible so that the recovery time required for the capacitor to return to its steady state condition will not interfere with the minimum pulse width

desired. In this case C_{in} recovers in about 0.2 μsec which is acceptable.

The value chosen for C_b is controlled by the choice of the transistors Q_1 and Q_2 as well as the minimum pulse width. It must be small enough to recover in about the same time or less than C_{in} does. However, it cannot be made so small that the input capacitance of Q_1 and Q_2 can cause a voltage division effect. When this happens, the gain of the regeneration loop is reduced and the flip-flop may fail to trigger when a pulse of short duration (such as that formed by C_{in}) is fed to the input. A value of $C_b = 4 \times C_{ob}$ is a reasonable value to use as an approximation for most transistors. Experimentation may yield a more optimum value but the above choice makes a good starting point. For the existing circuit, a value of C_b = 15 pf gives a satisfactory recovery time of about 0.1 μsec and is large enough to allow reliable operation.

The capacitor C_e is chosen so that the time constant R_eC_e is about 20 times the recovery time constants. A value of C_e = 0.01 μfd is sufficient for this circuit.

The flip-flop operated excellently in this application. Risetimes of about 0.05 μsec and pulse widths as short as 1/20 of a period (T_s = 5 μsec) were obtained without difficulty.

5.5 Chopper Design

Some important factors need to be considered in the design of a chopper for the intended application.

Purity of waveform is important. A waveform that has overshoots, ringing, or other imperfections that change with either amplitude or

pulse width will result in a degrading of linearity. A particular point to consider is changes in delay time that may occur with respect to amplitude or pulse width changes. In general, the output waveform desired is one that has a flat top and bottom, and edges that do not change their relative shape with changes in amplitude or pulse width.

Two types of choppers are discussed in this section; the double polarity chopper and the single polarity chopper.

(a) Double Polarity Choppers

(1) Diode Matrix Chopper

This type of switch was used in a vacuum tube version of the multiplier[2] that was to be converted to transistorized operation. The fundamental sweep frequency for the VT version was only 10 KHz but it was hoped that the circuit could operate at a frequency of 100 KHz or more with the use of fast diodes. The circuit is shown in Fig. 5.14.

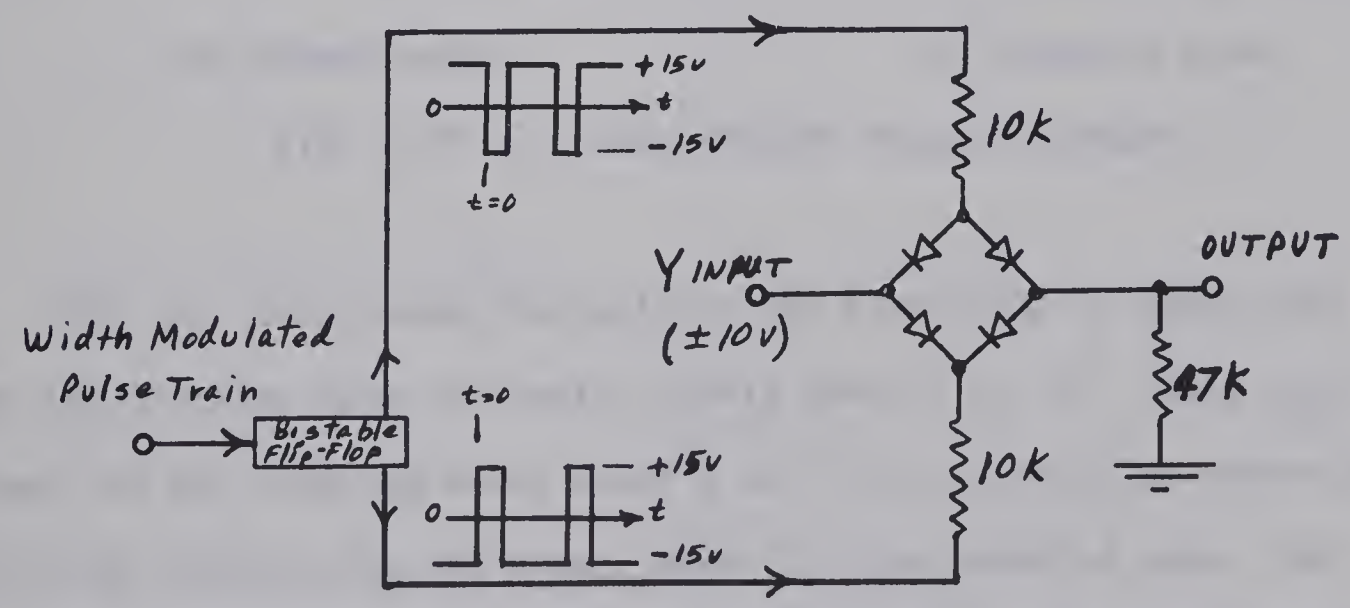


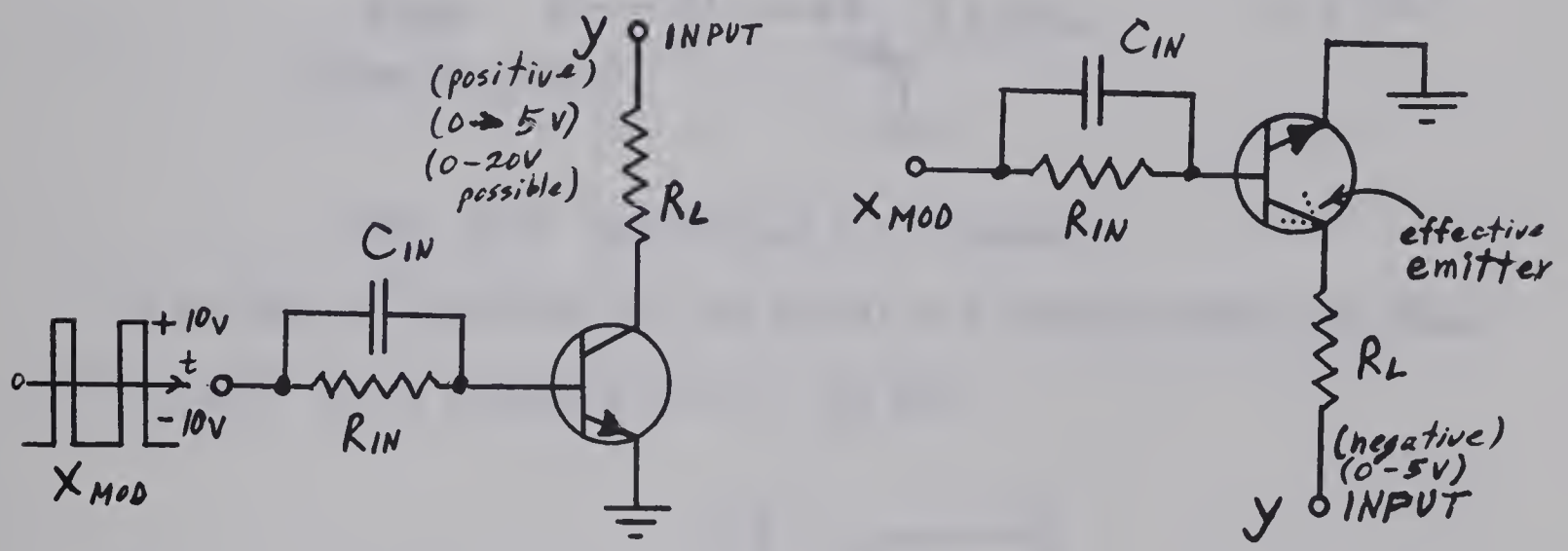
FIG. 5.14 Diode matrix chopper.

This circuit failed to show promise, the best risetimes obtained being in the 0.5 μsec range for recovery and the 0.1 μsec range for the

OFF to saturation condition. Although there was a chance for further improvement, the great difference between the speed of saturation of a diode and the speed of recovery made the use of this device unattractive. Thus it was decided to continue work on this device only if a better type of chopper could not be developed.

(2) Common Emitter Transistor Chopper

A single transistor used as a double polarity chopper in the common emitter configuration operates in two different modes as shown in Fig. 5.15.



(a) Normal mode. (b) Inverted mode.

FIG. 5.15 A common emitter chopper circuit.

For the normal mode, the gain of the transistor is about 100, but for the inverted mode, the gain is only about 5 or 10. Also, V_{CEO} is lower for the inverted mode, about 6 or 7 volts typically, rather than 25 to 30 volts as for the normal mode. In the inverted mode, the transistor operates as an emitter follower rather than a common emitter amplifier. Thus the driving pulse waveform must be more negative during its negative excursion than the most negative y signal voltage expected in order to be able to cut the transistor off.

After several experiments with input circuits to adjust for the two different gains in the two different modes (these modes result in two different input impedances), the simple circuit of Fig. 5.16 gave the most satisfactory performance.

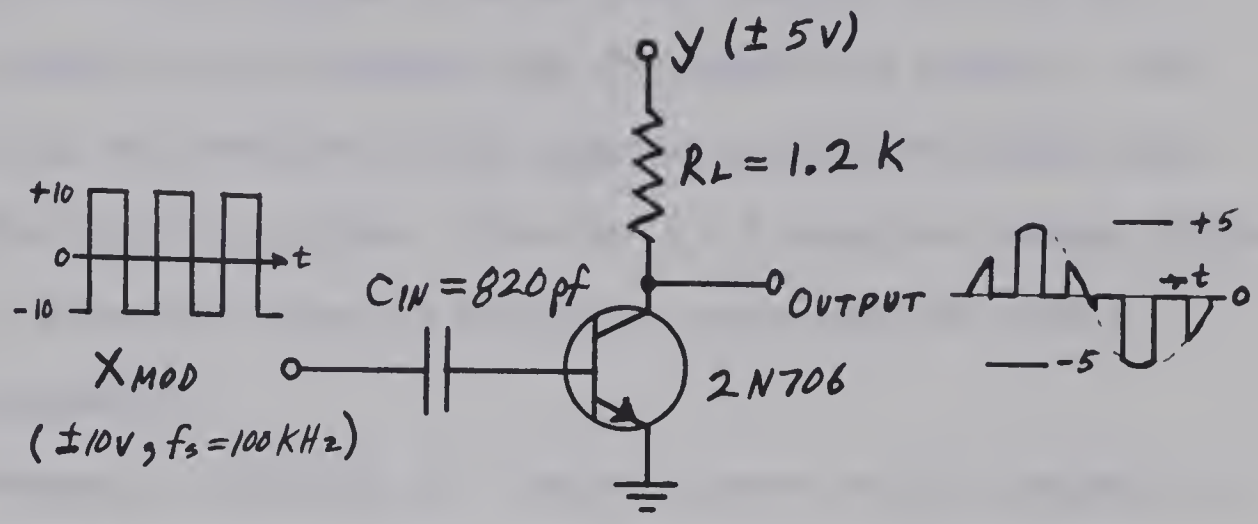


FIG. 5.16 Constructed C.E. chopper.

A variety of waveforms for the normal and inverted modes are shown in Fig. 5.17 for a frequency of f_s = 100 KHz.

(a) y = large, positive.

(b) y = small, positive.

(c) y = zero.

(d) y = small, negative.

(e) y = large, negative.

(not to scale)

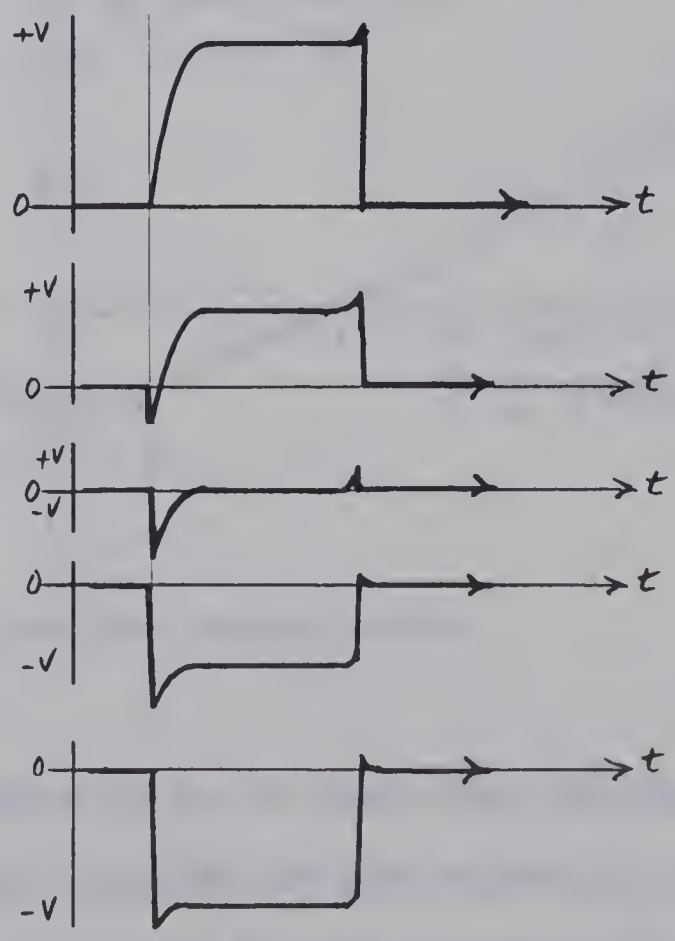
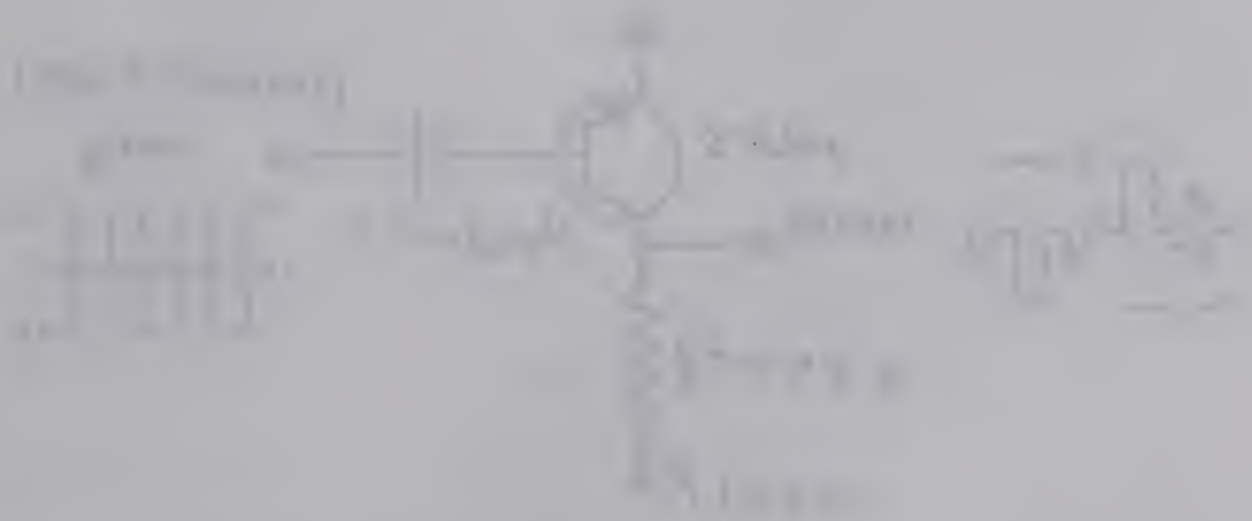


FIG. 5.17 Common emitter chopper waveforms.



As can be seen from the waveforms shown, there are various faults that affect the linearity of the amplitude modulation. The most obvious fault is the difference in risetimes of the leading edge when y is changed from a large positive value to a large negative value. This results in an effective change of pulse width causing the gain for positive y signals to be different than for negative y signals. Also noticed is that the overshoot on the negative y waveform becomes more pronounced for smaller y values. Even for y = 0 negative voltage spikes exist. For increasing values of positive y, this negative spike gradually disappears.

At a frequency of 100 KHz the linearity error of this chopper is in the order of 1 percent to 2 percent. This is mostly due to the change in gain effect mentioned previously. This can be seen in the shape of the deviation from linearity graph shown in Fig. 5.18.

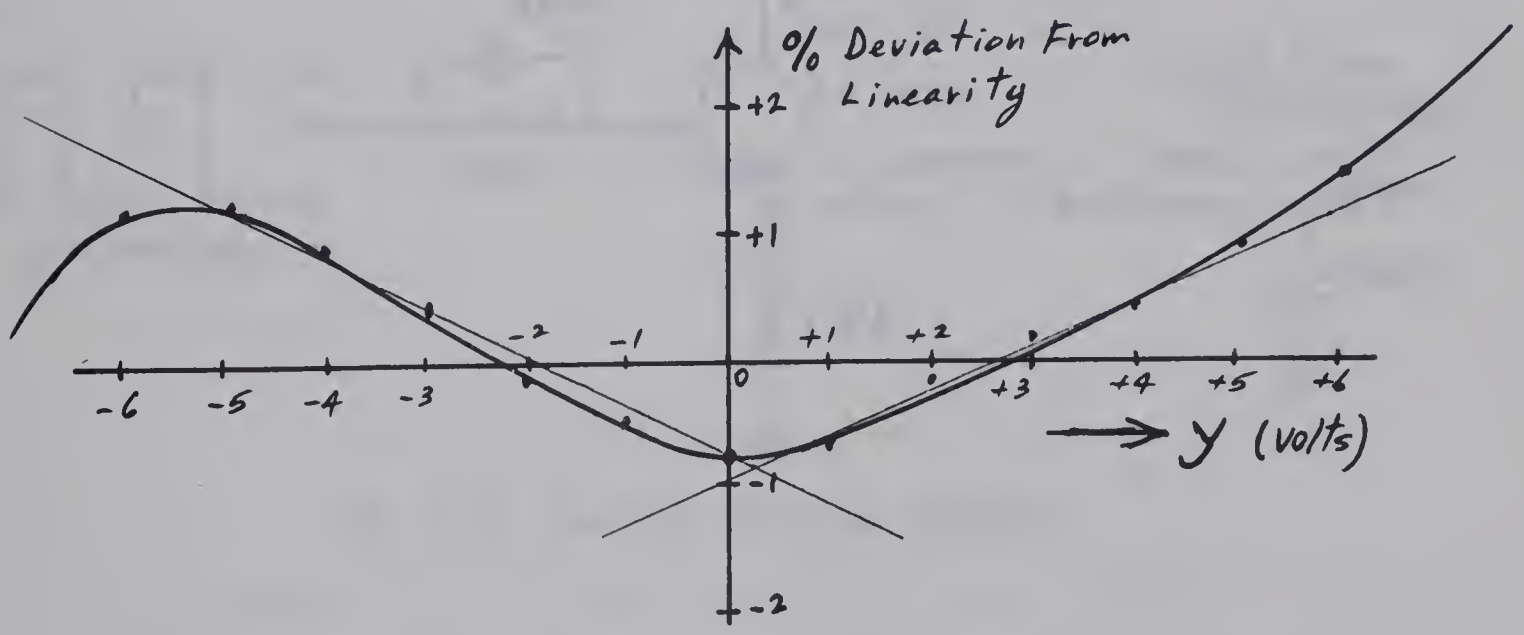


FIG. 5.18 Common emitter chopper error.

When the value of R_L is reduced to try to speed the risetime for positive y values (to equalize the risetime for each polarity), the driving current required from the bistable flip-flop becomes so large

that the flip-flop outputs become loaded down (even when emitter follower resistor values as low as 330 ohms are used).

Because of these basic problems with the double polarity chopper, a decision was made to study the feasibility of using only single polarity choppers to accomplish the required modulation. The result was the final circuit configuration discussed in section 4.2(a).

(b) Single Polarity Choppers

(1) Emitter Follower Chopper - (common collector).

The first single polarity chopper considered was the emitter follower chopper. This was due to the fast risetimes observed when the double polarity chopper was operating in the inverted mode as an emitter follower. The practical circuit developed is shown in Fig. 5.19.

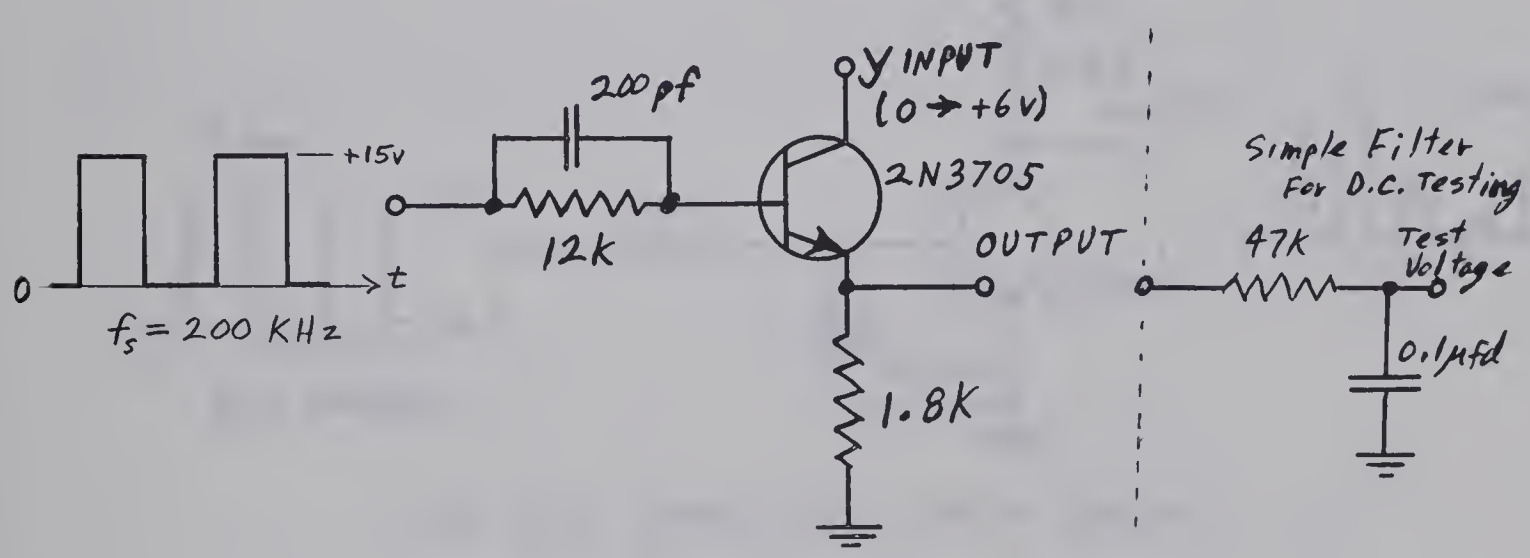
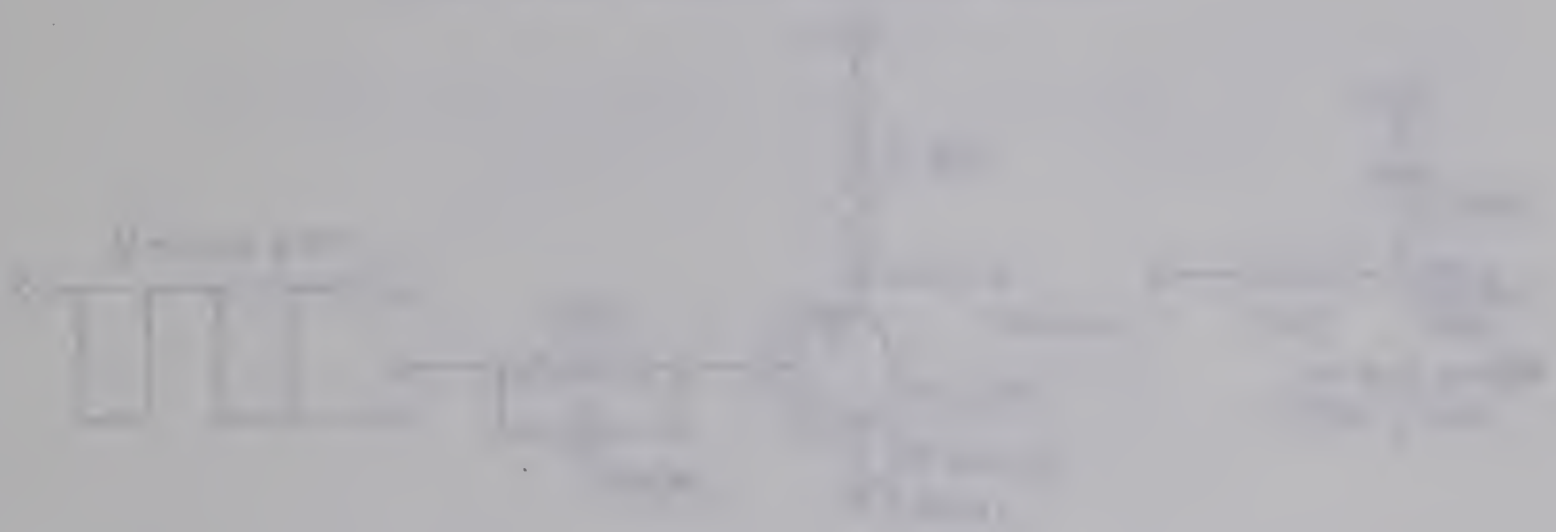


FIG. 5.19 Emitter follower chopper.

This circuit worked very well for the range of y = 1 volt to y = 6 volts giving a ±0.07 percent accuracy over the complete range. This is equivalent to a half range accuracy of ±0.14 percent. (See linearity test #10.) However, the error beyond the limits of the range increased rapidly. This makes it necessary to provide a reasonable



margin of safety in case two different choppers behave differently. As a result the input voltage signal would be restricted to about ±1.5 volts or ±2.0 volts at most. This was considered too limited for the intended use and the spike on the waveform was large enough to be objectionable; remembering that the linearity of width modulation could be affected by it.

(2) Tunnel Diode Hybrid Chopping Circuit

The success of the hybrid tunnel diode circuit in the width modulation circuit suggested the possibility that it could be used in a chopper application as well. The circuit of Fig. 5.20 was constructed to test this idea.

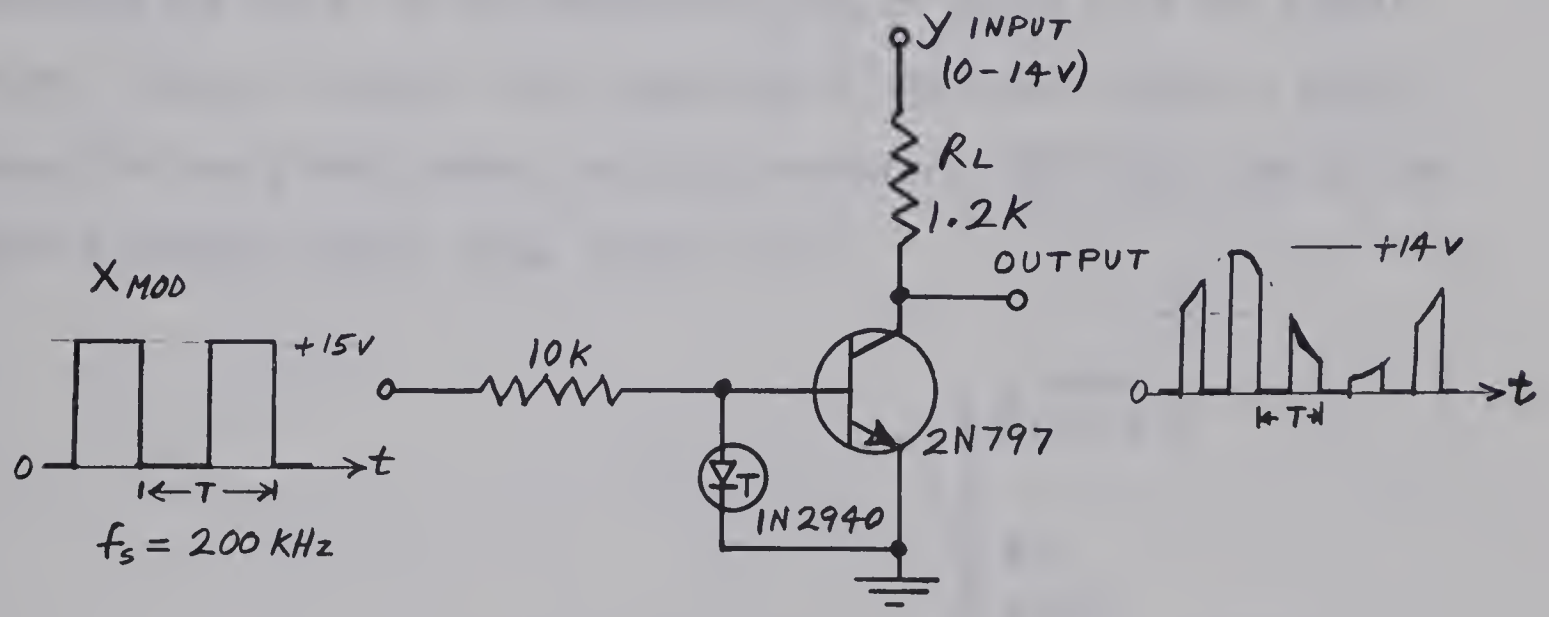


FIG. 5.20 Tunnel diode hybrid chopper.

The waveform obtained from this circuit was very good. There was only a relatively small negative spike noticeable for the case where y = 0. For positive values of y the spike disappeared and the waveform had no overshoot. When the pulse width was varied, the risetimes did not change noticeably and quite narrow pulses were easily obtained. The linearity obtained from this chopping circuit was about ±0.07 percent

over the range of y voltages from 0 volts to +14 volts. The equivalent error for the half range is about ±0.14 percent. Even better accuracy is possible if the input voltages are limited to the range between 2 volts and 10 volts.

For these reasons, this circuit was used to construct the amplitude modulator section of the multiplier. The only change made in the circuit finally used was to replace the germanium 2N797 transistor with the silicon 2N3705 transistor. This resulted in a lower saturation voltage (about 40 mv rather than 90 mv) and a smaller change in saturation voltage with change in the y signal voltage. As mentioned in section 5.1(c), the use of a silicon transistor in the hybrid circuit requires the use of an OA5 germanium diode in series with the tunnel diode. Also, to ensure fast triggering of the tunnel diode, a small capacitor was placed across the input resistor. The final form of the hybrid chopper used is shown in Fig. 5.21.

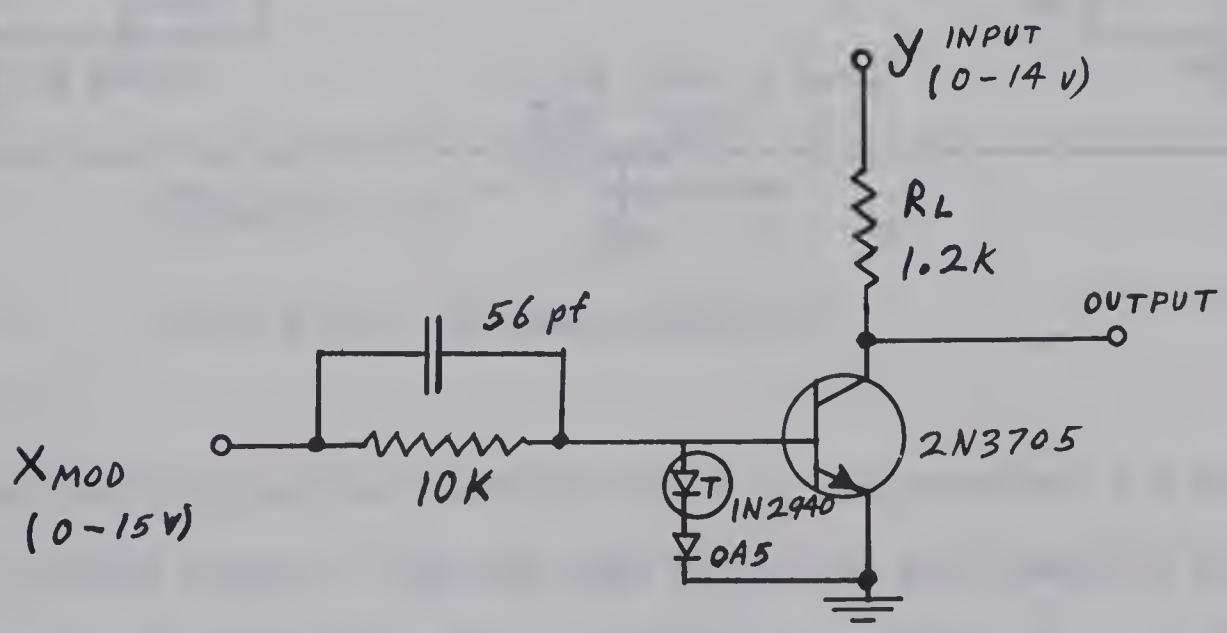


FIG. 5.21 Final hybrid chopper circuit.

5.6 Amplitude Modulator

Using the configuration discussed in section 4.2(a) (Fig. 4.6) and the tunnel diode chopper developed in the previous section, an amplitude modulator circuit was constructed. The circuit as tested is shown in Fig. 5.22.

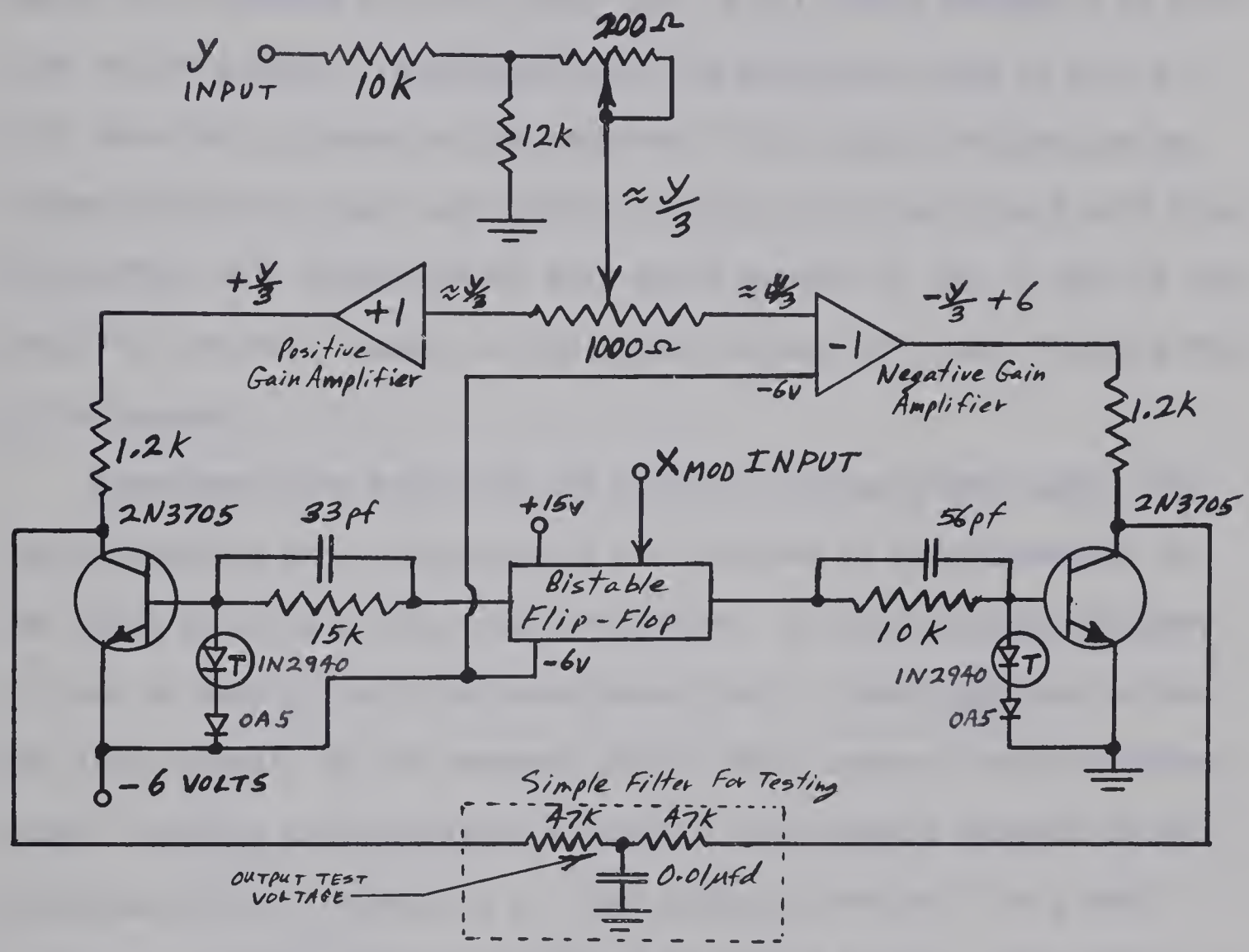


FIG. 5.22 Amplitude modulator.

The two 47 K ohm resistors and the 0.01 μfd capacitor are not part of the circuit itself. They are used to provide the summation and simple filtering for testing of the circuit. This circuit performed well enough (see linearity test #11) to incorporate it into the final design.

A potential source of trouble is the stability of the negative 6 volt power supply. A variation of this supply would result in an

undesired change of output if the problem had not been compensated for. The effect of the supply variation is offset by using this negative 6 volt supply voltage to provide the positive 6 volt bias for the signal at the output of the inverting amplifier. As shown in Fig. 5.22, this is done by using the supply as one of the inputs to this negative gain amplifier. Because of the -1 gain, the -6 volt input becomes a +6 volt bias at the output. Investigation of the waveforms shown in Fig. 4.7 will show that a change in the negative 6 volt supply voltage can be compensated by an equal but opposite change in the positive 6 volt bias. This effect will automatically take place because of the -1 gain of the amplifier and thus changes of the supply voltage will have little effect on the output.

Adjustments for balancing the gains of the two signal paths (and for controlling the y signal gain) are provided by potentiometers in the input circuits of the input amplifiers. An input voltage divider is used to obtain the 1/3 attenuation of the y signal required to keep the input signals to the choppers within their chosen linear operating range. Because the saturation voltage of the choppers depends on the magnitude of the y signal to a slight extent, there will be a small residual y signal existing in each of the pulse trains. This effect is not bothersome as it can be cancelled out by adjustment of the input balancing potentiometer just mentioned.

The design of the input amplifiers for the amplitude modulator is dealt with in the next section.

5.7 Input Operational Amplifier Design

Three input buffer amplifiers are required for use in the multiplier. Operational amplifiers are preferred to simple emitter followers because of their superior linearity and temperature performance. These amplifiers were designed and constructed as part of the multiplier to prevent tying up analog computer amplifiers and to avoid the risk that the computer amplifiers might be unsuitable for use with the multiplier. Built-in amplifiers also provide the convenience of using the multiplier for applications external to the analog computer.

(a) General Operational Amplifier Design

The basic operational amplifier circuit used for the input amplifiers is shown in Fig. 5.23.

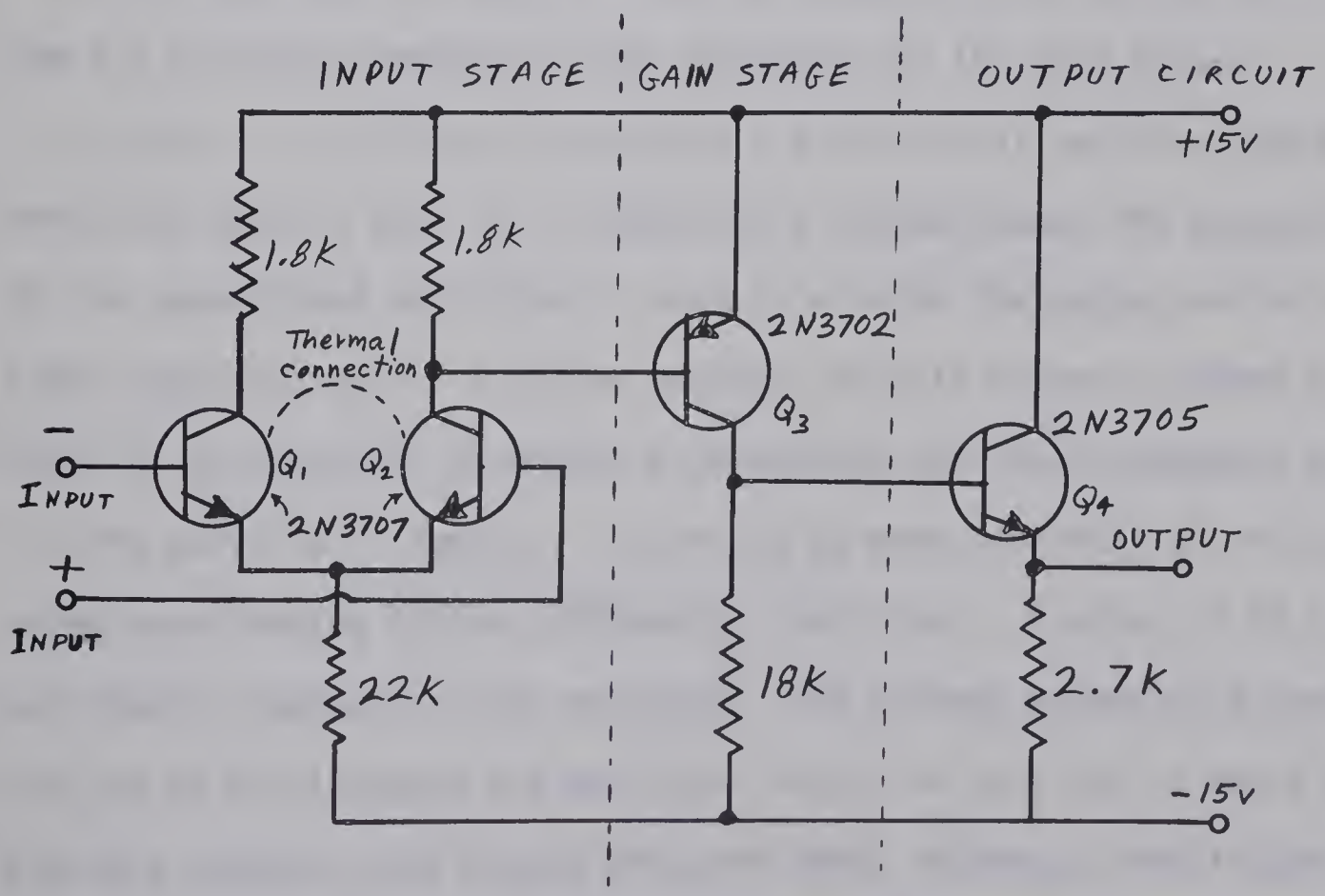


FIG. 5.23 Basic operational input amplifier.

The circuit shown uses the minimum number of components required to accomplish its task. The differential amplifier input circuit is a standard circuit for achieving low temperature drift. The two transistors (Q_1 and Q_2) in this stage should be matched at the nominal operating current such that their base-emitter voltages agree within 1 mv or 2 mv and their current gains agree within about 20 percent. They also should be thermally connected to keep their operating temperatures as close as possible. An operating current of about 340 μa for each transistor is provided by the 22 K ohm resistor. The h_{ib} of each transistor at this current will be about 80 ohms. This current is slightly high to achieve optimum drift performance but necessary because of the limited number of stages. A resistor instead of a current source was used to provide the bias current because extremely low common mode gains were not required for the amplifiers in this application. A load resistor of 1.8 K ohms is used to provide the 0.6 volt bias needed for the transistor of the next stage.

Since it is difficult to obtain a differential amplifier gain of more than about 5 when it is loaded by a second stage, the second stage of the operational amplifier is used to provide the major portion of the total amplifier gain. The load resistor of this stage is chosen as small as is practical to ensure a reasonable open loop frequency response for the amplifier. However, it can not be made too small as this would cause more loading of the differential amplifier. A value of 18 K ohms was finally chosen for this resistor. The voltage across this resistor will be 15.6 volts when the amplifier output is zero (as it would be with the feedback loop closed and zero input voltage). This is due to the 0.6 voltage drop across the base-emitter junction of the output

emitter follower transistor Q_4. A resulting quiescent current of 0.87 ma will flow in transistor Q_3 . The h_{ib} of the transistor can be calculated for this current as

$$h_{ib_3} \simeq \frac{26 \times 10^{-3}}{I_e} = \frac{26}{0.87} = 30 \text{ ohms} .$$

The input impedance of this stage is given as

$$Z_{in_3} \simeq h_{fe}\, h_{ib} = 100 \times 30 = 3.0 \text{ K ohms} .$$

This input impedance does not load the output impedance of the differential stage (1.8 K ohms) too seriously. The expected gain of this stage will be

$$A_{v_3} \simeq \frac{R_L}{h_{ib}} = \frac{18 \text{ K}}{30} = 600 .$$

The measured gain of the stage was about 630.

With the input impedance of the second stage approximated, the gain of the differential stage can be computed. The gain equation is given as

$$A_v = \frac{R_L}{2\, h_{ib} + R_s/h_{fe}}$$

R_L = load resistance of input stage (effective)
R_s = source resistance
h_{ib} = h_{ib} of input transistors.

Then for the inverting amplifier of Fig. 5.34 (using approximate values)

$$A_{v_1} = \frac{(1.8\text{K})(3.0\text{K})/(1.8\text{K} + 3.0\text{K})}{160 + 5\text{K}/200} \simeq 6 .$$

This gives a total amplifier gain (open loop) of A = 6 x 600 = 3600. The measured gain was about 3500.

The last stage of the amplifier provides the low output impedance required for the intended application. It must be able to supply output

currents up to about 10 ma. A simple emitter follower biased at a quiescent current of 6 ma (by choosing an emitter resistor value of 2.7 K ohms) proved to be suitable for all three amplifiers required. The current gain of this stage is about 100. This will result in an open loop output impedance for the amplifier of about 3.0 K ohms. When the loop is closed as in a unity gain inverter the output impedance is significantly reduced. It can be calculated by using the expression

$$Z_{of} = \frac{Z_o}{1 + A} = \frac{3.0\ K}{3600} = 0.84 \text{ ohms} .$$

Even with such a low output impedance a problem occurred with transient voltage spikes on the output due to the ON-OFF current demand of the amplitude modulator. This effect was minimized by providing high frequency filtering in the amplifier and is discussed later for each input amplifier.

The amplifier was capable of a full output of ±5 volts to a 1.2 K ohm load at frequencies ranging to 300 KHz. The distortion caused by the amplifier was almost unmeasurable with the equipment used but was of the order of 0.05 percent or less up to 5 KHz.

(b) Input Amplifiers for the "y" Signal Paths

The circuit configuration in which the positive and negative input amplifiers are used is shown in Fig. 5.24. Two of the basic amplifiers just discussed are used with resistor networks that produce positive unity gain and negative unity gain. The gain of 1/3 required to attenuate the y signal to a value within the range of the chopping circuits is produced by a voltage divider at the input of the two amplifiers. Potentiometer P_1 provides gain adjustment for the y signal

and potentiometer P_2 provides adjustment for balancing the gain of the two y signal paths through the chopping circuits. The negative gain amplifier is used to provide the +6 volt bias that is required in its signal path. The bias is produced by connecting an amplifier input resistor to the negative 6 volt power supply. Potentiometers P_3 and P_4 provide coarse and fine adjustments of the bias level.

Both the positive and negative amplifiers were stable without a load attached which is surprising for a 4 transistor operational amplifier without frequency compensation. Spontaneous oscillation is not unexpected in amplifiers of this type. However, large voltage transients appeared on the amplifier outputs when they were connected to the amplitude modulator. Thus filtering to produce extra feedback at high frequencies is required to eliminate these transients. The filtering was obtained by placing a 15 pf capacitor from the base to the collector of the input transistor of each amplifier. This is Q_1 for the negative gain amplifier and Q_2 for the positive gain amplifier. The completed amplifiers are shown in Fig. 5.34. In the amplifiers, the transient spikes were reduced to an acceptable value of ±100 mv in magnitude. The ringing that accompanies the spikes dies out fast enough to avoid affecting the width modulation linearity.

The temperature drift of the amplifiers is about 0.5 mv/^{o}C or about 0.3 mv/^{o}F (see temperature test #6). This is about 0.01 percent/^{o}F for the magnitude of signal used with these amplifiers and is quite acceptable.

The only other problem that had to be considered with the amplifiers was the change in output that can occur when the input of an amplifier is changed from a floating to a grounded state. The change can result

from the voltage offset of the amplifier (due to differing input transistor V_{be} voltages). The problem is minimized by using an input voltage divider to obtain a 1/3 gain (rather than making $R_f/R_{in}=1/3$). With this input circuit, grounding the input represents a much smaller change of source impedance than occurred previously. The problem is now completely eliminated by placing a 2K ohm potentiometer in the load resistor circuit of the input differential stage of the negative gain amplifier (as shown in Fig.'s 5.35 and 5.36). This potentiometer is adjusted until the voltage at the ungrounded input becomes zero. Now, grounding this input will have no effect.

The amplifier performance is now considered very satisfactory.

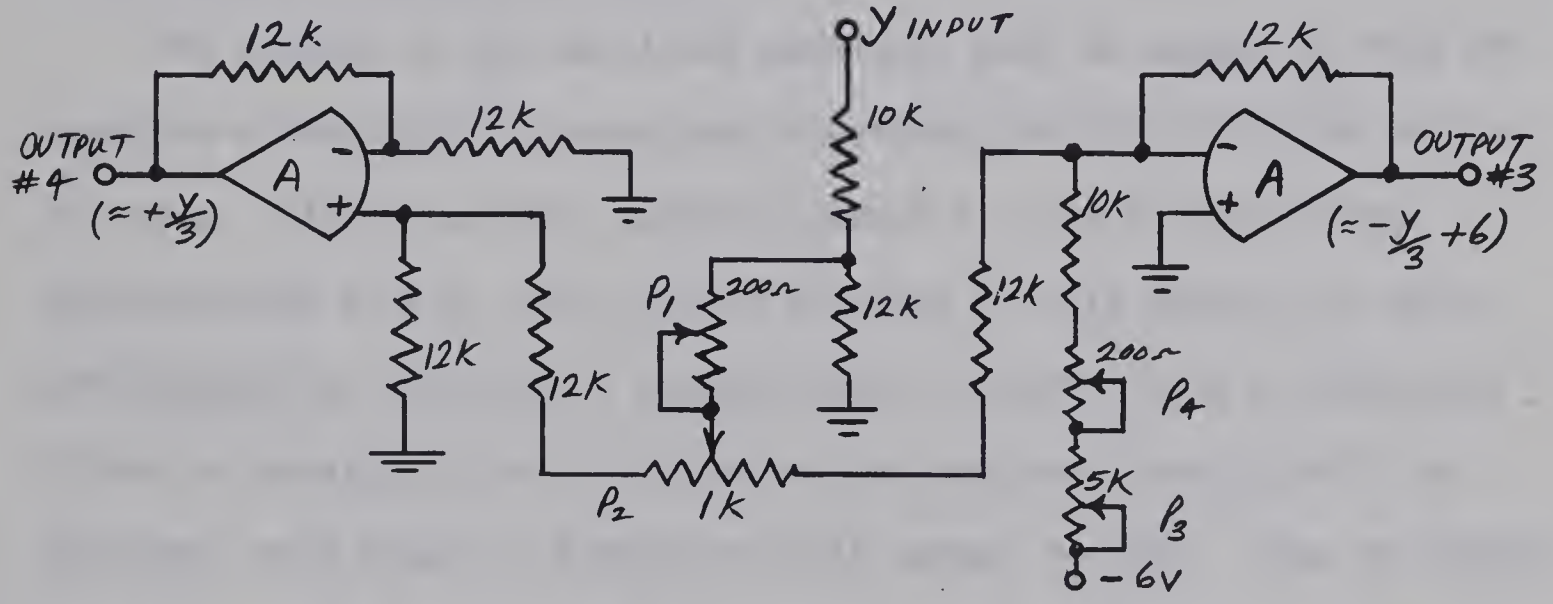
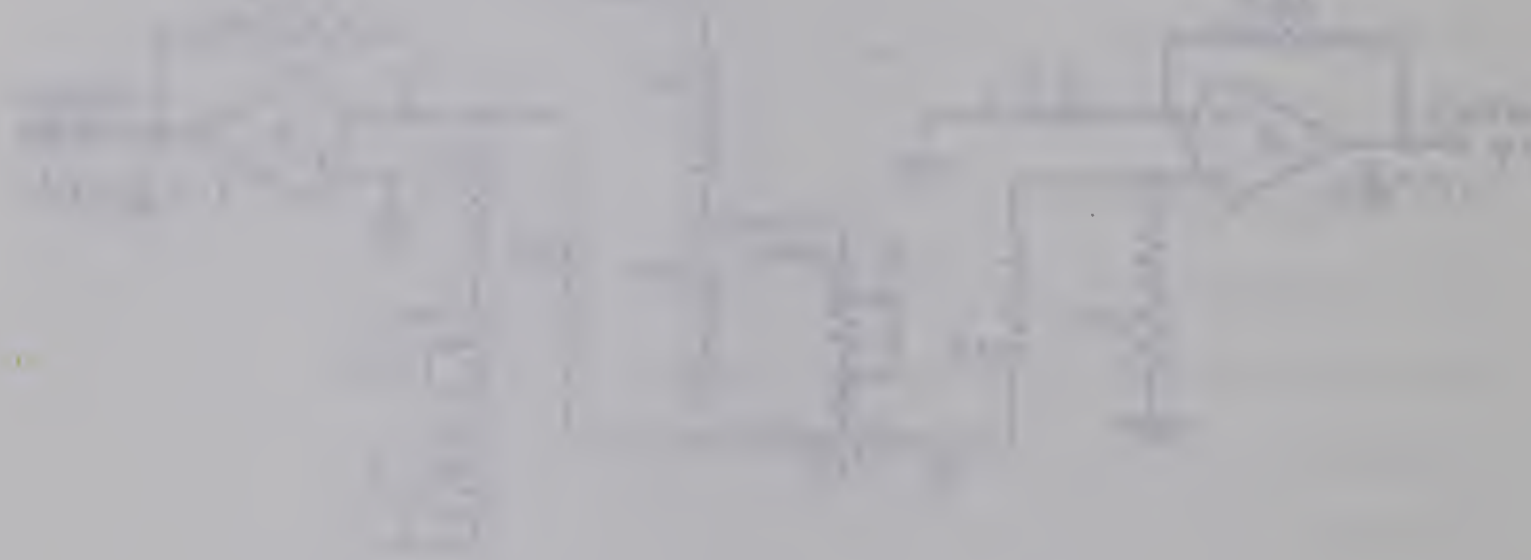


FIG. 5.24 Input amplifier circuit configuration for the "y" signal paths.

(c) Input Amplifier for the "x" Signal Path

The inverting amplifier just discussed in section 5.7(b) is also suitable for this purpose. The configuration in which the amplifier is used is shown in Fig. 5.25. The voltage divider (which gives a 0.5 gain) and a 2K ohm potentiometer put in the differential input stage are



used for the same reason as mentioned previously.

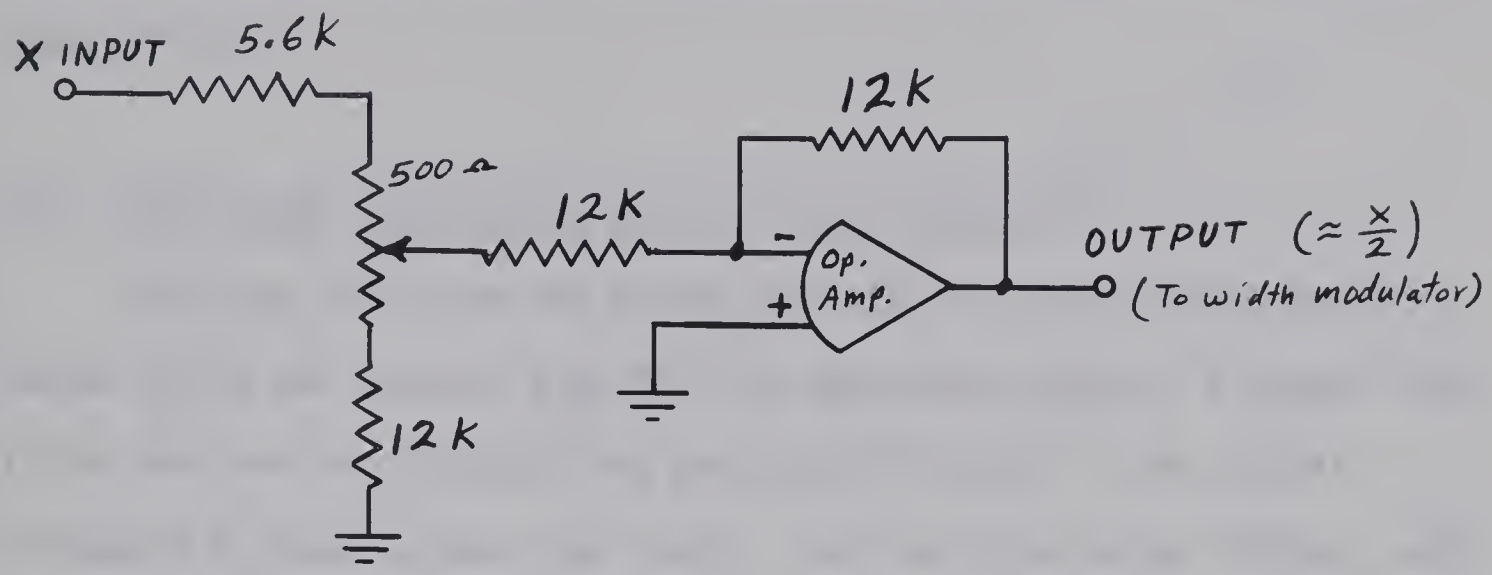
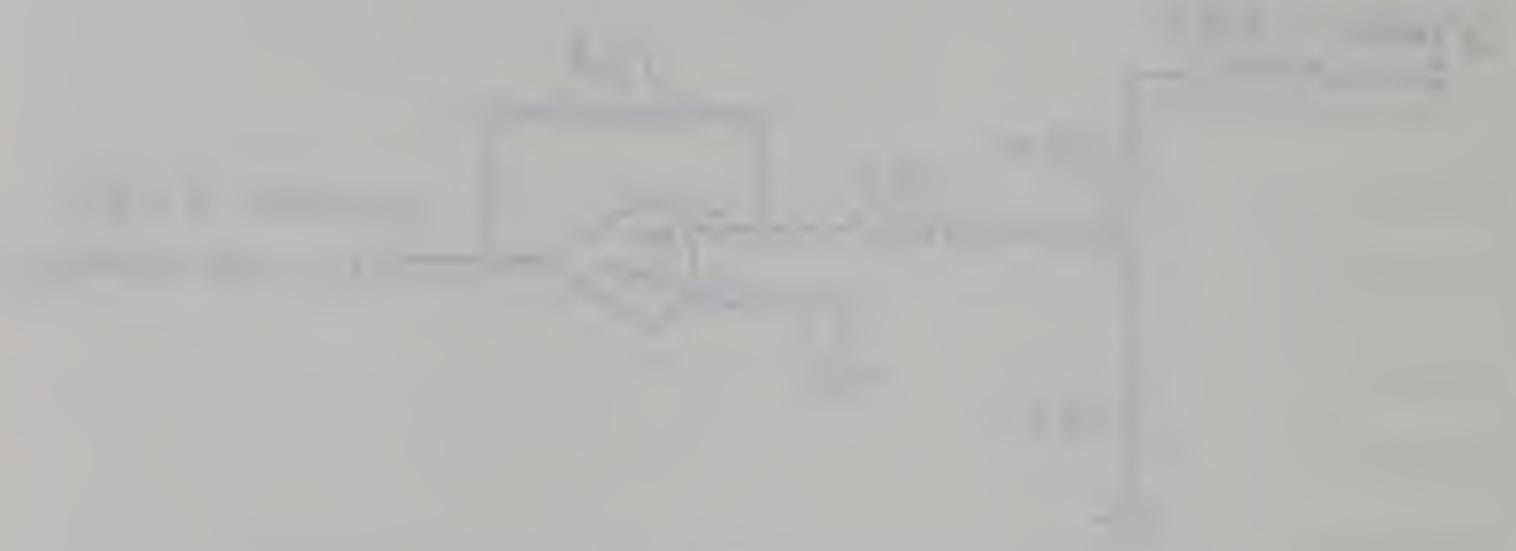


FIG. 5.25 Input amplifier for "x" signal path.

5.7 Output Amplifier and Filter

The outputs of the amplitude modulator must be summed to form the complete width-amplitude modulated waveform, and then this sum must be filtered. With a resistor summing network as used in the circuit configuration of Fig. 5.22, output voltages of only about ±1.5 volts are obtained at the network output (after filtering with a unity gain filter or passive filter). To ensure the desired linearity will be obtained, only about ±1.0 volts of this output is used. Thus an output gain of about 10 is required to produce a ±10 volt output. It was decided to combine the filter and gain of -10 amplifier to make a low pass active filter with a gain of -10 in the band-pass region. If an active filter followed by an amplifier of a -10 gain was used, the drift of the filter would be amplified by a factor of 10. Combining the two features in one device minimizes the temperature drift problem.

The type of active filter used was the third order Butterworth filter[5]. Because of the gain of -10 and the need for large values of



resistors in the input to avoid loading of the amplitude modulator outputs, more care was needed in the design of the amplifier in the active filter.

(a) Third Order Butterworth Active Filter Design[5]

This type of filter was chosen for its relatively sharp cut-off (about 60 db per decade) and its flat band-pass region. A higher order filter was not used because the phase shift at the -3 db cut-off frequency f_c then becomes too large. For the third order filter, this phase shift is about 135^o. The filter design shown in Fig. 5.26 was obtained from reference (5) and has a unity gain in the band-pass region. Modification to produce a gain of 10 is discussed later in this section.

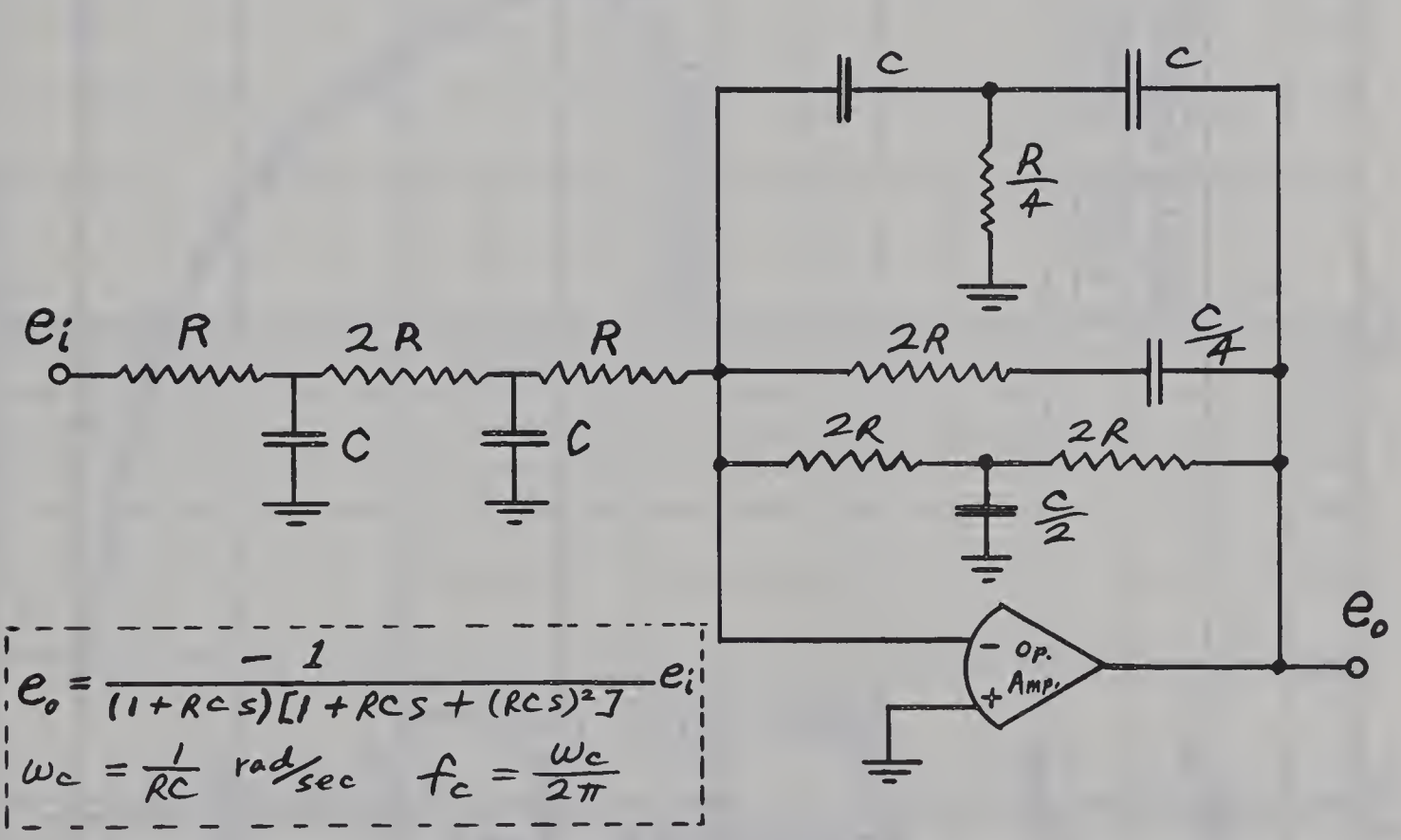


FIG. 5.26 Third order Butterworth active filter.

The cut-off frequency of the filter required to properly demodulate the width-amplitude modulated pulse train was discussed in section 3.3.

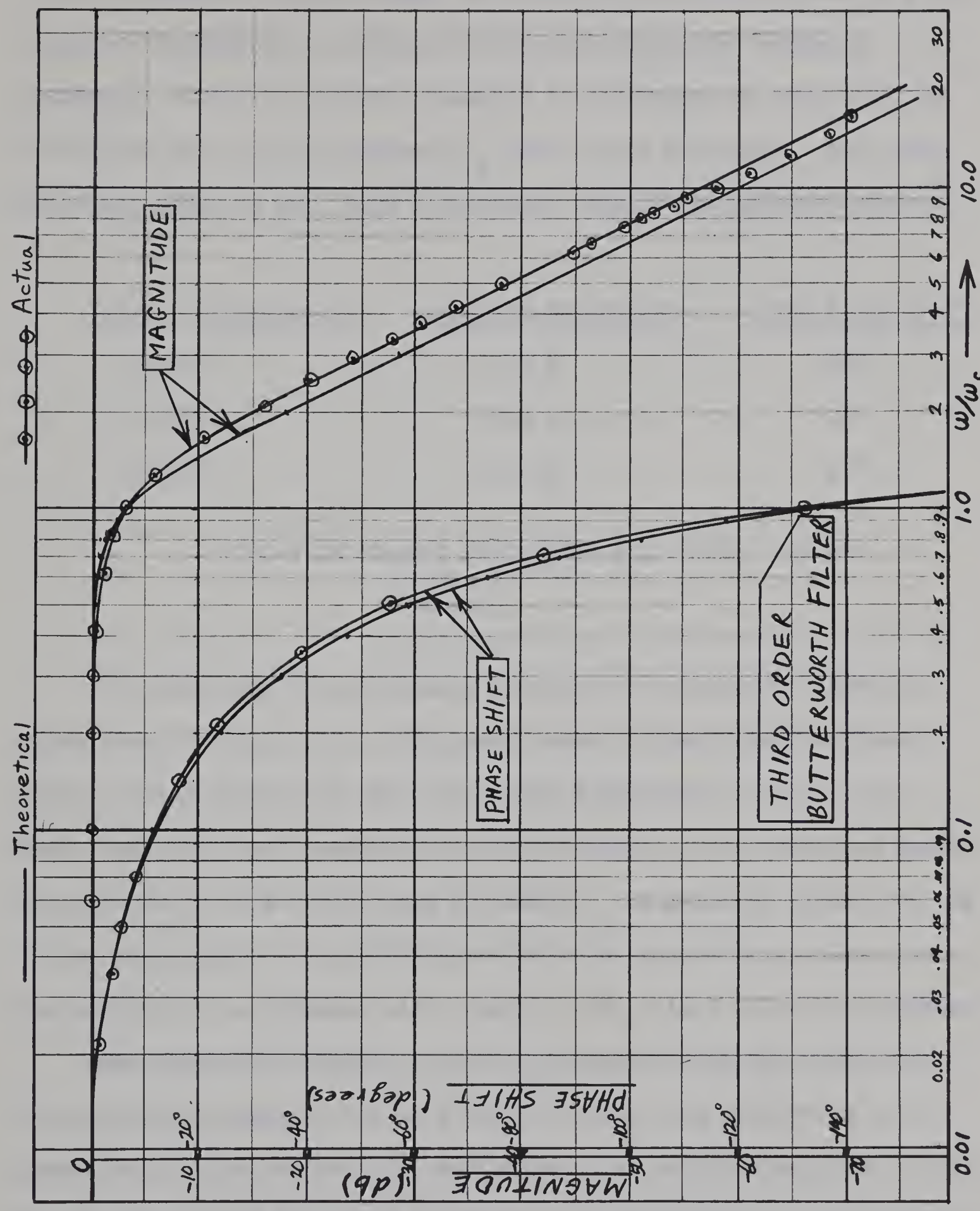


FIG. 5.27 Magnitude and phase shift of the third order Butterworth filter VS normalized frequency $\frac{\omega}{\omega_c}$.

It was discovered that the major portion of the distortion due to high frequency components is produced by the 200 KHz pulse frequency component. Thus the cut-off frequency is determined by the amount of distortion due to this component f_s that can be tolerated. The table of values shown in Fig. 5.28 illustrates some of the possible choices.

Cut-off Frequency f_c	Expected Distortion	5 KHz Phase Shift
15 KHz	0.1 %	36^o
22 KHz	0.3 %	24^o
25 KHz	0.5 %	22^o

FIG. 5.28 Output distortion V.S. filter cut-off frequency.

The values for Fig. 5.28 were obtained by calculation from the graph shown in Fig. 5.27. This graph shows the magnitude and phase shift characteristics of the third order Butterworth active filter. Both theoretical and measured results are shown on the graph and these prove to be in relatively close agreement. The measured values for the filter were used in Fig. 5.28 rather than the theoretical values since the multiplier performance will depend on the actual filter performance.

When making the choice of cut-off frequency from the results in Fig. 5.28, the emphasis can be placed on either low distortion or low phase shift. For the existing multiplier, the decision was made to use the 15 KHz cut-off frequency to obtain a low distortion. If the phase shift of 36^o at 5 KHz is too large for a particular application, a different cut-off frequency can be used. Since the multiplier is built on modular printed circuit boards, a change of cut-off frequency is

just as simple as unplugging one filter-amplifier and plugging in another. A series of boards for different applications could be built if so desired.

If the filter input was connected to the output of the amplitude modulator shown in Fig. 5.22, the filter characteristics would be altered by the impedance of the resistor summing network. The proper characteristics are preserved by embodying the summing function into the filter's first input resistor. This input resistor is replaced by two input resistors which form a summing network. Each of the resistors must be made twice the value of the original input resistor so that their parallel resistance equals the value of the original input resistor. In this way, the original filter characteristics are retained. Another possible solution to the problem would have been to build two identical input networks for the filter and essentially perform the summation at the amplifier summing junction. This would effectively double the signal strength to the amplifier resulting in a lower required gain of 5 for the amplifier. However, the matching of the components to obtain perfectly matching phase shift characteristics of the two networks would be too difficult to make this solution practical.

As mentioned previously, the filter design of Fig. 5.26 must also be modified to produce a gain of 10 rather than the unity gain it has. To do this, the resistors in the feedback network are increased by a factor of 10. To retain the same cut-off frequency, the capacitors in the feedback network must then be reduced by a factor of 10. The new filter configuration is illustrated in Fig. 5.29.

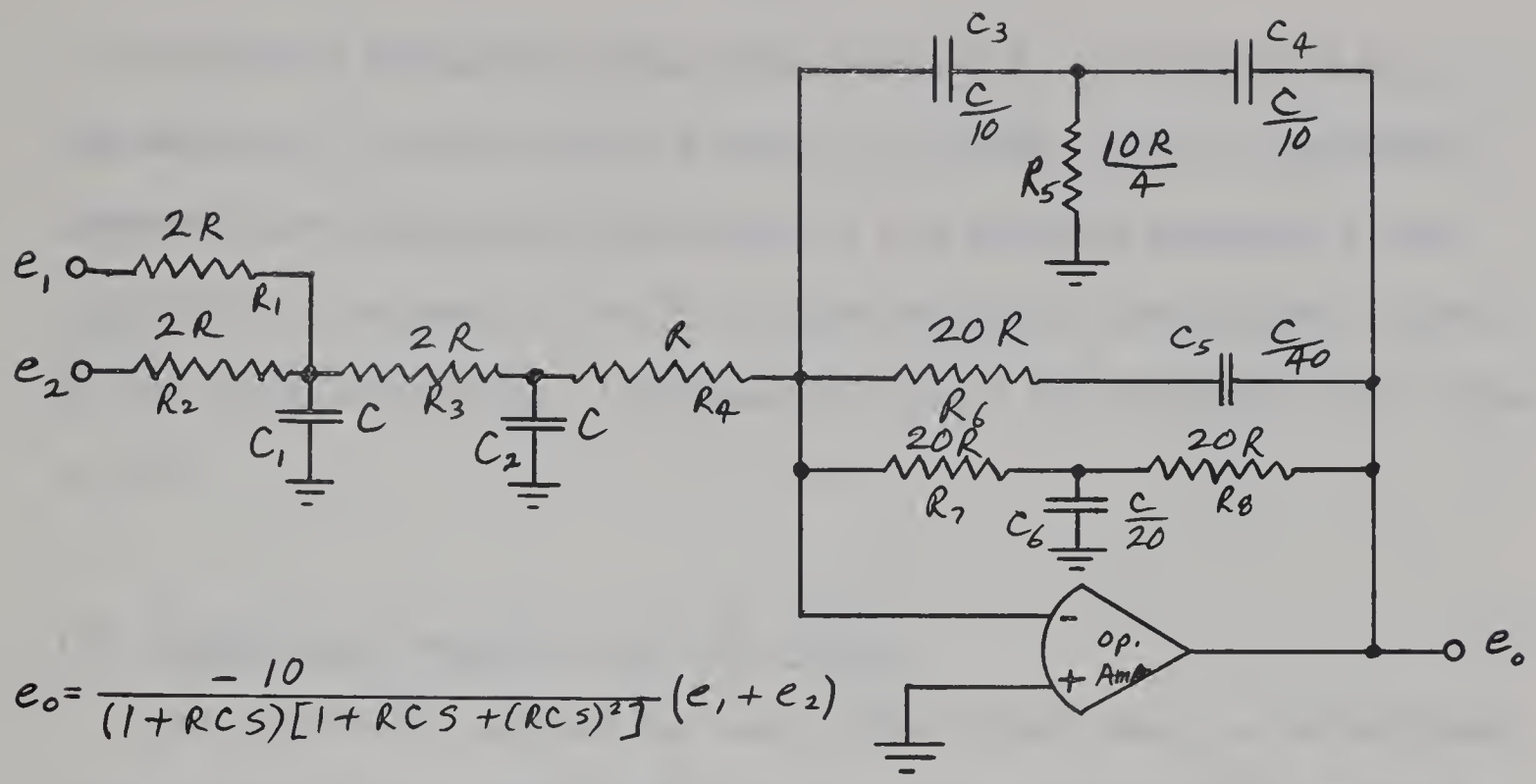


FIG. 5.29 Modified Butterworth active filter.

The value of 2R can be made as small as 22 K ohms without seriously loading the amplitude modulator outputs. The proper value of R then is 11 K ohms, but a standard value of 12 K ohms is used without serious error. Computation of the remaining filter values can procede. The value of capacitor C is calculated to be

$$C = \frac{1}{2\pi f_c R} = \frac{1}{(6.28)(11\times10^3)(15\times10^3)} = 965 \text{ pf.}$$

The standard value used for C is 1000 pf. Although not exact, this value allows the other capacitor values to be chosen as standard values as well. The component values chosen for the filter are listed below:

$R_1, R_2, R_3 = 2R = 22$ K ohms,
$R_4 = R = 12$ K ohms,
$R_5 = 10R/4 = 27$ K ohms,
$R_6, R_7, R_8 = 20R = 220$ K ohms,

$C_1, C_2 = C = 1000$ pf,
$C_3, C_4 = C/10 = 100$ pf,
$C_5 = C/40 = 25$ pf,
$C_6 = C/20 = 47$ pf.

With this choice of values, the expected f_c is about 14.5 KHz. The measured f_c of the actual filter is 14.0 KHz. This is reasonable agreement considering the tolerances of the standard components used (typically 10 percent). The f_c is close enough to the desired value of 15 KHz to be acceptable. The phase shift at 5 KHz for the actual filter is 39^o.

(b) Operational Amplifier for the Filter

The amplifier required for use in the filter needs to be designed more carefully than those used for the inputs. Because the amplifier will be used with a gain of -10 rather than -1 the corresponding open loop gain must also be larger to retain a similar performance level with regard to distortion and output impedance. The output circuitry needs to be protected against short circuits since users of the multiplier will be connecting the output to other circuits and accidental shorts are possible. More care must be taken with frequency responses within the amplifier also because of the higher impedance levels of the feedback and input networks.

The amplifier shown in Fig. 5.30 was adapted from a circuit suggested by a member of the faculty of the Electrical Engineering Department.

Originally, the standard two transistor differential amplifier input stage was used in the amplifier. However, the gain of a simple stage like this is not very high and drift in the second stage of the amplifier referred to the input was as large or larger than the drift of the input stage. To make the second stage drift negligible, the gain of the input stage was increased by replacing each of the

transistors of the differential amplifier with a complementary compound connected transistor pair. This results in an actual differential amplifier gain of 45.

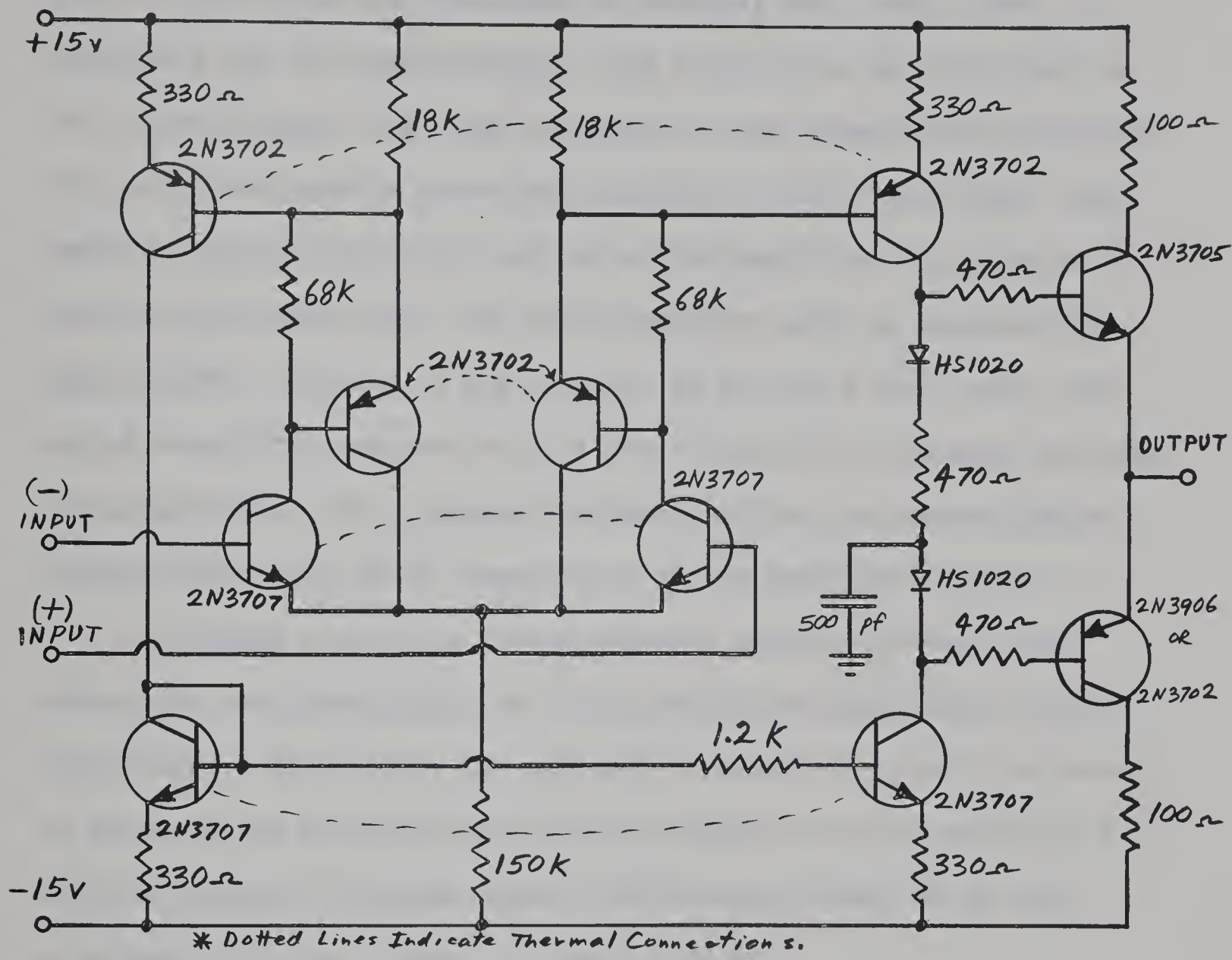


FIG. 5.30 High gain operational amplifier.

The second stage of the amplifier is designed to drive a complementary emitter follower output circuit. The bases of the output transistors are connected to the collectors of a complementary pair of common emitter amplifiers. Two silicon diodes and a resistor are connected between these collectors to bias the quiescent current of the output circuit. The PNP common emitter amplifier is driven directly by

one output of the differential amplifier and the NPN common emitter amplifier is driven by a unity gain inverter connected to the other differential amplifier output. Each C.E. amplifier acts as a current source to the other and thus each effectively has a very large resistance for its load resistor. The result is a very high gain in this second stage. The input impedance of the output circuit degrades this gain to a certain extent but the gain is still very high. The measured gain of this stage for use of the amplifier in a gain of 10 inverter was about 1100. The total amplifier gain was measured as about 50,000. Because of the symmetry of the two signal paths, the output transistors are driven by signals of similar frequency and phase characteristics. This reduced the opportunities for unpredictable instabilities and makes compensation of the amplifier simpler.

The output circuit is a complementary emitter follower with protection resistors placed in the collector and base leads of the transistors. This limits the collector currents for shorts to ground to about 150 ma which the transitors can take for short periods. A 470 ohm resistor is placed between the biasing diodes to set the quiescent collector currents at about 0.25 ma.

To achieve low drift, the input NPN transistors are operated at about 9 μa each and should be matched at this current for equal V_{be} voltages and h_{fe} current gains. The PNP transistors of the input stage operate at about 39 μa so they should not contribute appreciably to the temperature drift. The symmetry of the amplifier allows four pairs of transistors to be thermally connected for V_{be} drift cancellation. The actual measured drift of the amplifier was not as good as expected but was not objectionable (voltage drift =.003 percent/^{o}F).

The amplifier is unstable without some form of frequency compensation. The best position found to apply the frequency compensation was at one end of the biasing resistor (ie. the 470 ohm resistor between the two biasing Si diodes at the input of the output stage). A 500 pf capacitor connected from this point to ground produced a high frequency roll-off of 20 db per decade and was sufficient to stabilize the amplifier for full output without causing appreciable phase shift in the operating frequency range. Distortion due to the amplifier was almost unmeasurable, being of the order of 0.05 percent or less.

A zeroing network was necessary to adjust for the voltage offset of the amplifier and to adjust for the offset voltage of the amplitude modulator. The offset of the modulator is slight but when amplified by a gain of 10 is large enough to require adjustment for. A coarse adjustment and a fine adjustment are provided for as shown in the final completed filter-amplifier of Fig. 5.36.

The performance obtained from this filter-amplifier was more than sufficient for the application in the multiplier.

5.9 Design of the Negative 6 Volt Power Supply

A total of three power supplies are required to operate the multiplier. To avoid the need to use more than two commercially purchased supplies, the -6 volt supply is derived from the -15 volt supply by the voltage regulator circuit of Fig. 5.31.

The supply uses a common emitter series regulator circuit. The feedback amplifier consists of the standard differential configuration but the zener reference diode is used in an unusual manner. The normal

way to connect the reference diode is from the base of Q_1 to ground. The bias resistor then would be connected to the -6 volt supply voltage or to the -15 volt supply if it was reasonably regulated. Comparison of the reference voltage with the output voltage is realized by using a voltage divider from the output to the base of Q_2. Regulator action will result in a voltage at the base of Q_2 equal to the reference voltage. Changing the divider ratio changes the output voltage needed to keep the base of Q_2 at the reference voltage. Thus by adjusting the divider ratio the desired -6 volt output can be obtained. The difficulty that occurs when this method is used is that if the zener voltage is of a reasonably large value (ie. zeners of 5.6 volts or more have sharper "knees"), then the ratio of the voltage divider is so low that the loop gain is reduced by a large amount. A much higher loop

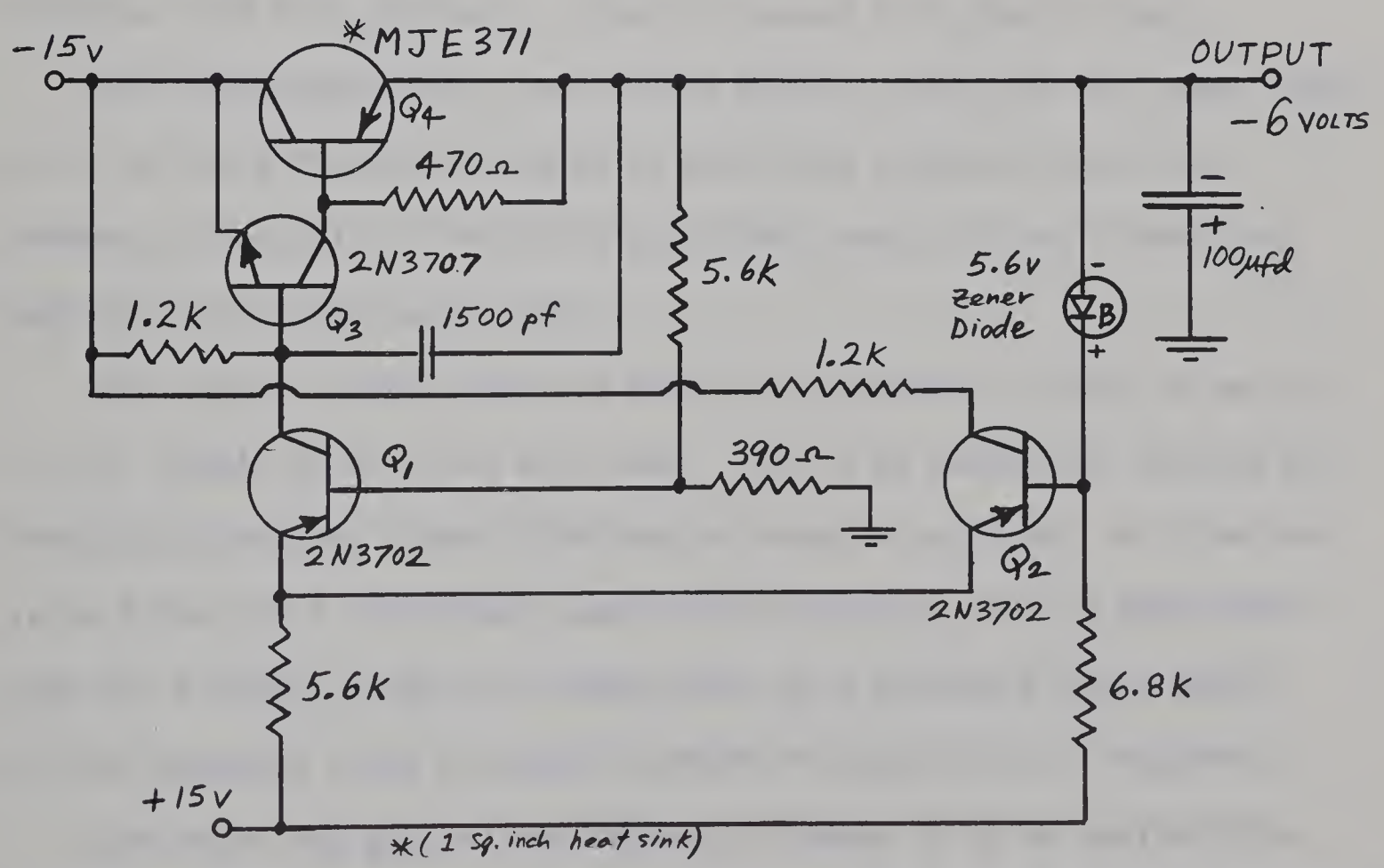


FIG. 5.31 Negative 6 volt power supply.

gain is produced when the output voltage change is transmitted directly to the base of Q_2 by the zener diode as shown in Fig. 5.31. When the base of Q_1 is connected to ground the output voltage is regulated to the value of the zener diode. Larger value output voltages can be obtained by connecting a voltage divider from the output to the base of Q_1 and to ground (see Fig. 5.31). When the voltage divider is adjusted such that the output voltage is only slightly higher than the value of the reference diode then the divider ratio is so low that only a slight loss of regulation results. In this case the zener voltage is 5.6 volts and the output voltage is 6.0 volts so the regulation is reduced by only about 7 percent. To produce a high loop gain, the series regulator element consists of a complementary compound connected transistor pair that acts as a single high gain transistor. The output impedance obtained from this regulator circuit is about 0.03 ohms or less.

The temperature drift performance depends mainly on the zener diode drift as the differential amplifier gives the regulator itself an inherently low drift. The drift is of the order of 2 mv/^{o}F which is negligible for this application.

The output current required from the regulator is about 30 ma but it will supply up to 70 ma with ease. For 70 ma operation, the MJE 371 transistor requires a heat sink area of about 1 sq. inch. An aluminum strip ½ inch by 2 inches was used in the prototype, but an equivalent area (or slightly larger) of copper-clad on a printed circuit board will be suitable since an actual current of only 30 ma is required.

The high loop gain of the regulator causes it to be unstable for light loads. The high frequency oscillation that results can be stopped by reducing the loop gain for high frequencies. A 1500 pf capacitor

connected from the collector of Q_1 to the output stabilizes the regulator.

The regulator as constructed gives very good performance for the specialized application in this multiplier.

5.10 Elimination of Noise Pickup in the Multiplier

When the complete multiplier was put into operation, numerous switching spikes appeared at the multiplier output, on the power supply leads in various circuits, and other parts of the multiplier. These caused such problems as making the operation of the multiplier sensitive to the body capacitance of a person who placed his hand close to the circuitry. Various solutions to eliminate this pickup problem were implemented.

(a) Capacitor Decoupling

Elimination of switching spikes on power supply leads was obtained wherever necessary by placing a large value of capacitance in these positions as close to the operating circuitry as possible. The various capacitors used are indicated in the circuits 5.32 to 5.37.

(b) Use of Printed Circuit Boards

Further elimination of pickup was difficult at first because the circuits had been built on vector boards using components with long leads, long wire connections between circuits, and haphazard circuit arrangement in general. Thus the decision was made to immediately transfer the circuitry to printed circuit boards (which eventually would be done in any case). Circuits were arranged as logically as possible

on the boards and they were constructed to plug into a rack containing the necessary interconnections. The improvement of the pickup problem was better than expected with the switching spikes on the output and other circuit parts almost entirely removed.

(c) Use of Shielding Between Boards

A small further improvement was noticed when the output filter-amplifier was shielded from the other circuit boards with a grounded sheet of aluminum. Even though no difference was noted, the other operational amplifiers in the multiplier technically should be shielded also because of the high gains involved.

At this point, the problem of pickup for a single multiplier is considered to be solved.

5.11 Multiplier Power Supply Requirements

Two commercial power supplies are necessary to operate the multiplier; one + 15 volt supply and one - 15 volt supply. The required specifications are described as follows:

(a) Current Output. The supplies should be capable of a current output of 150 ma per multiplier (an actual 100 ma is needed).

(b) Output Impedance. The output impedance should be as low as possible to avoid spikes on the supply voltage due to sudden current demands. This impedance should stay low for high frequencies also. A value of about 0.05 ohms should be suitable.

(c) Stability. The supplies should be stable with respect to time and temperature. A total deviation of more than ±100 mv is undesirable.

They should also be adjustable to allow setting of the voltages to exactly 15 volts in magnitude.

(d) Operation With More Than One Multiplier

There is a possibility of interaction occurring when two multipliers are operated from the same set of supplies. The seriousness of the problem is unknown at this time but interaction sufficient to cause degraded performance is not expected. If the reverse is found to be true, then separate supplies or methods of isolation and shielding must be used.

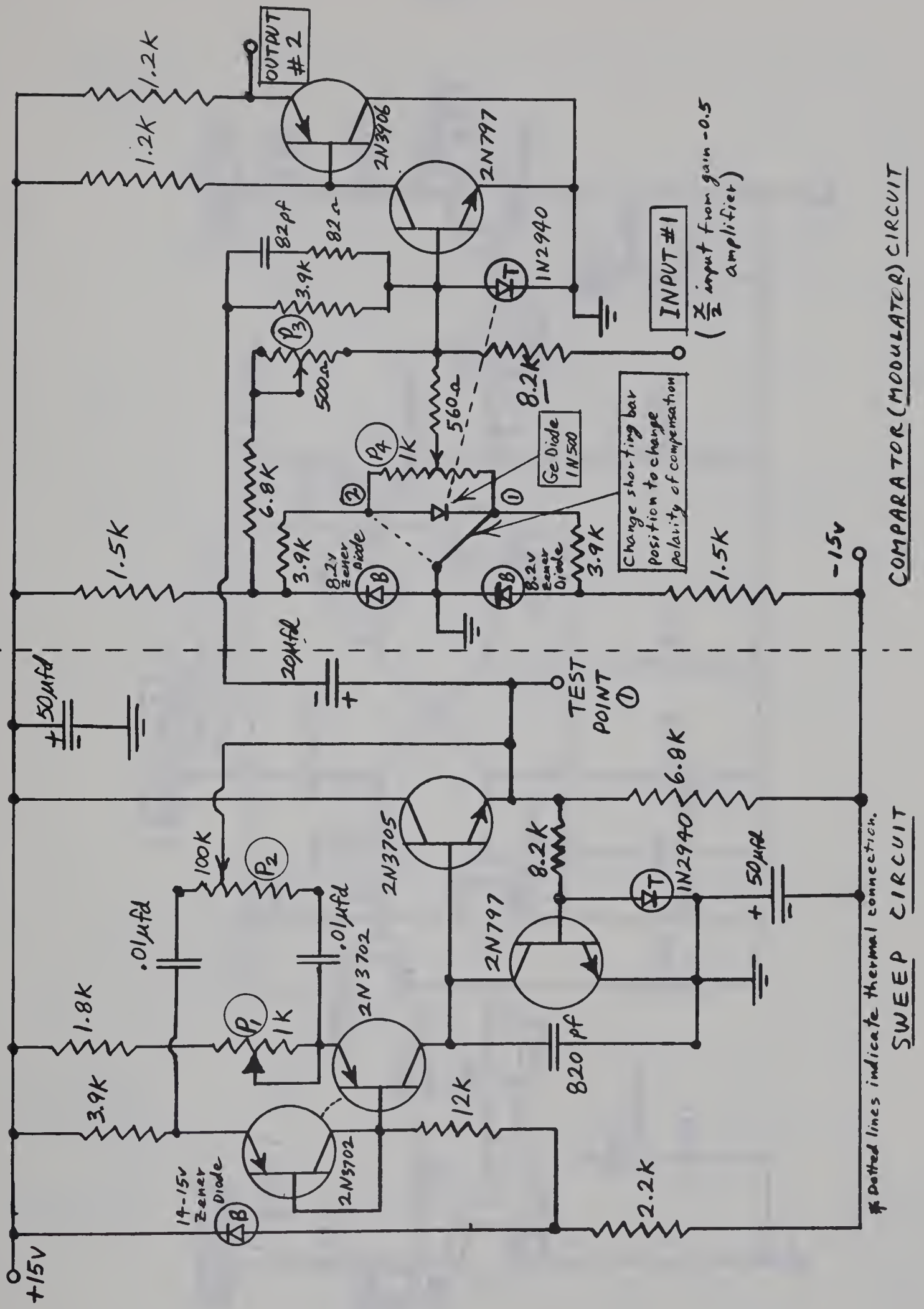
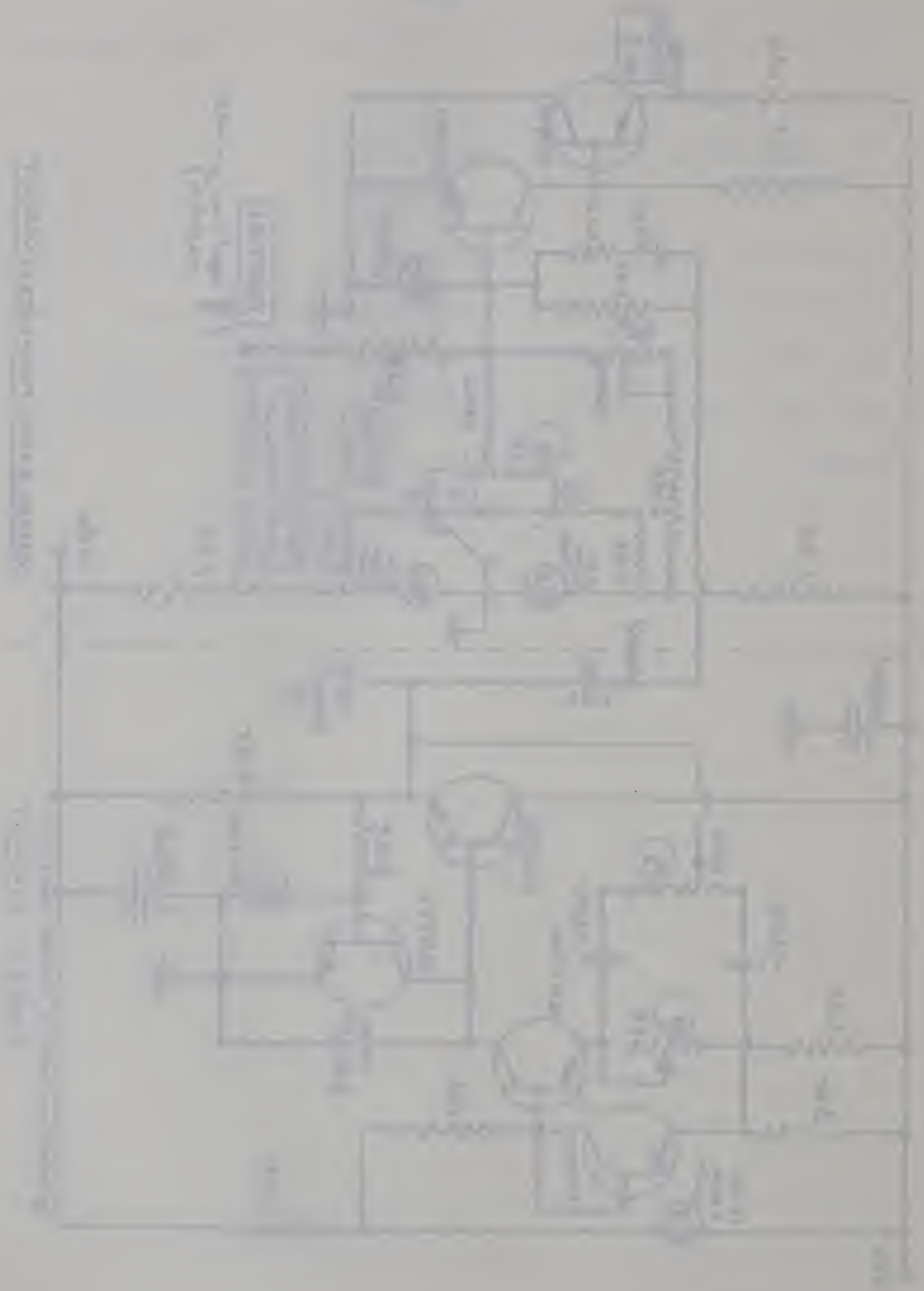


FIG. 5.32 Pulse width modulator.



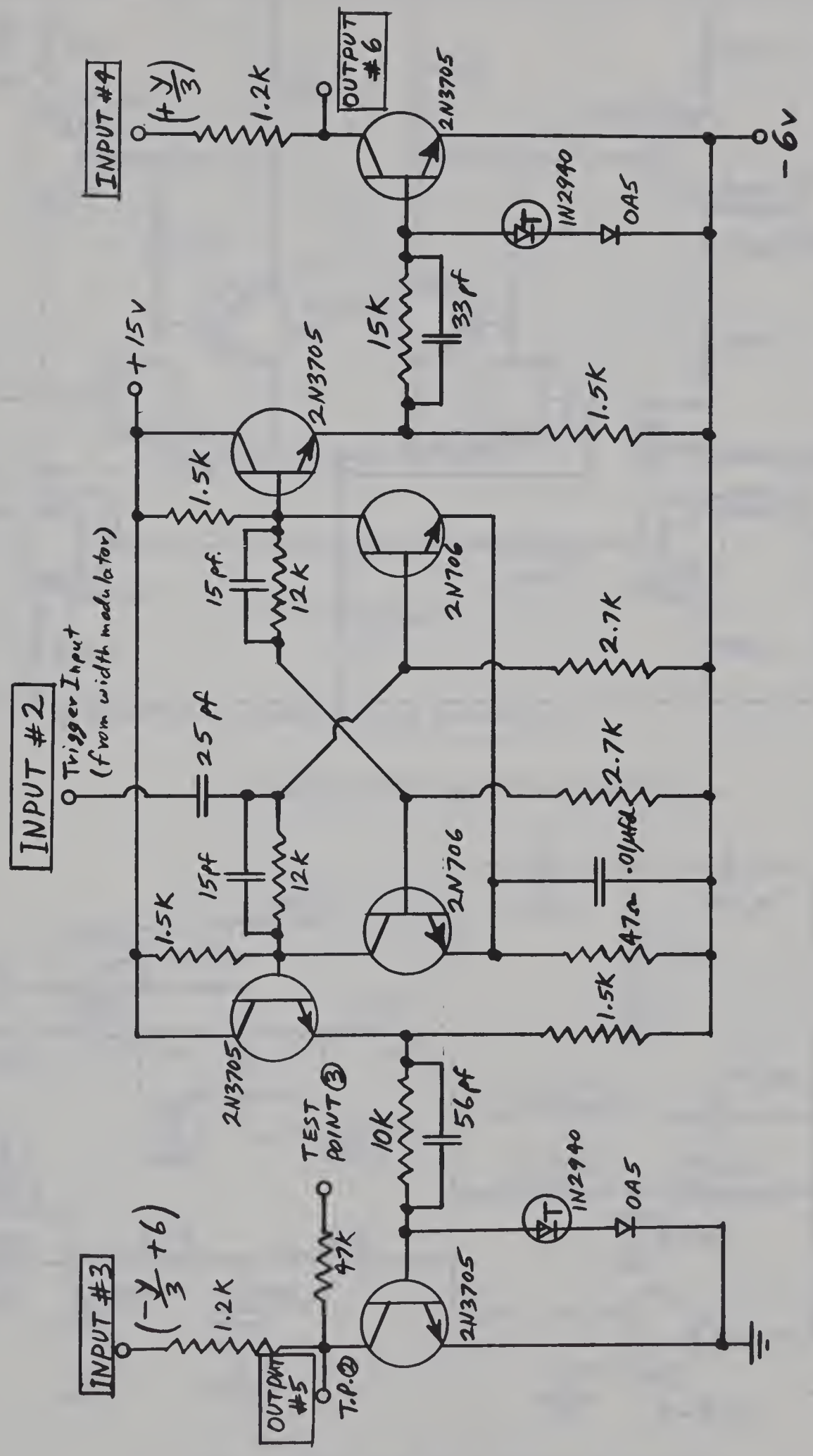
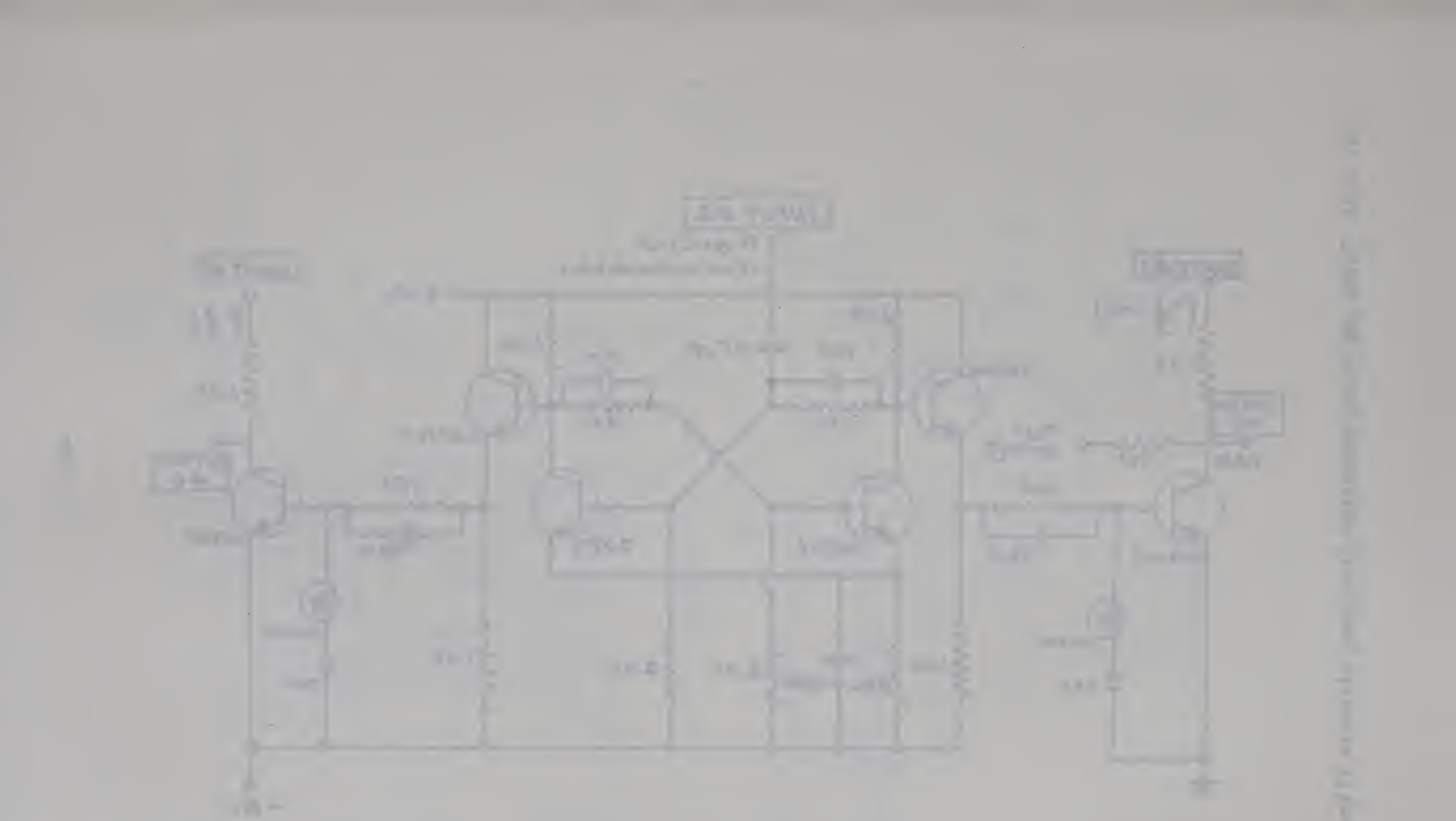
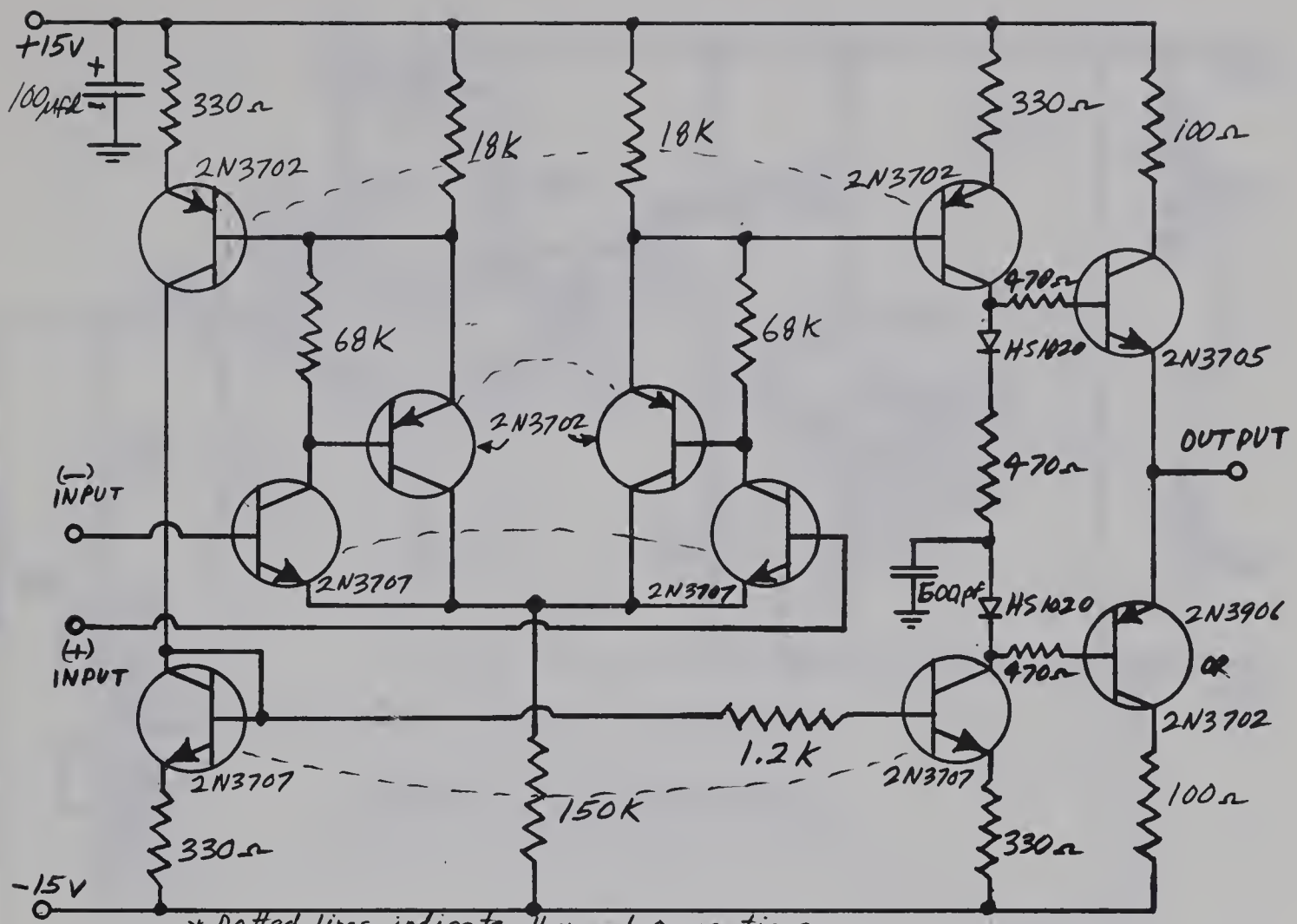
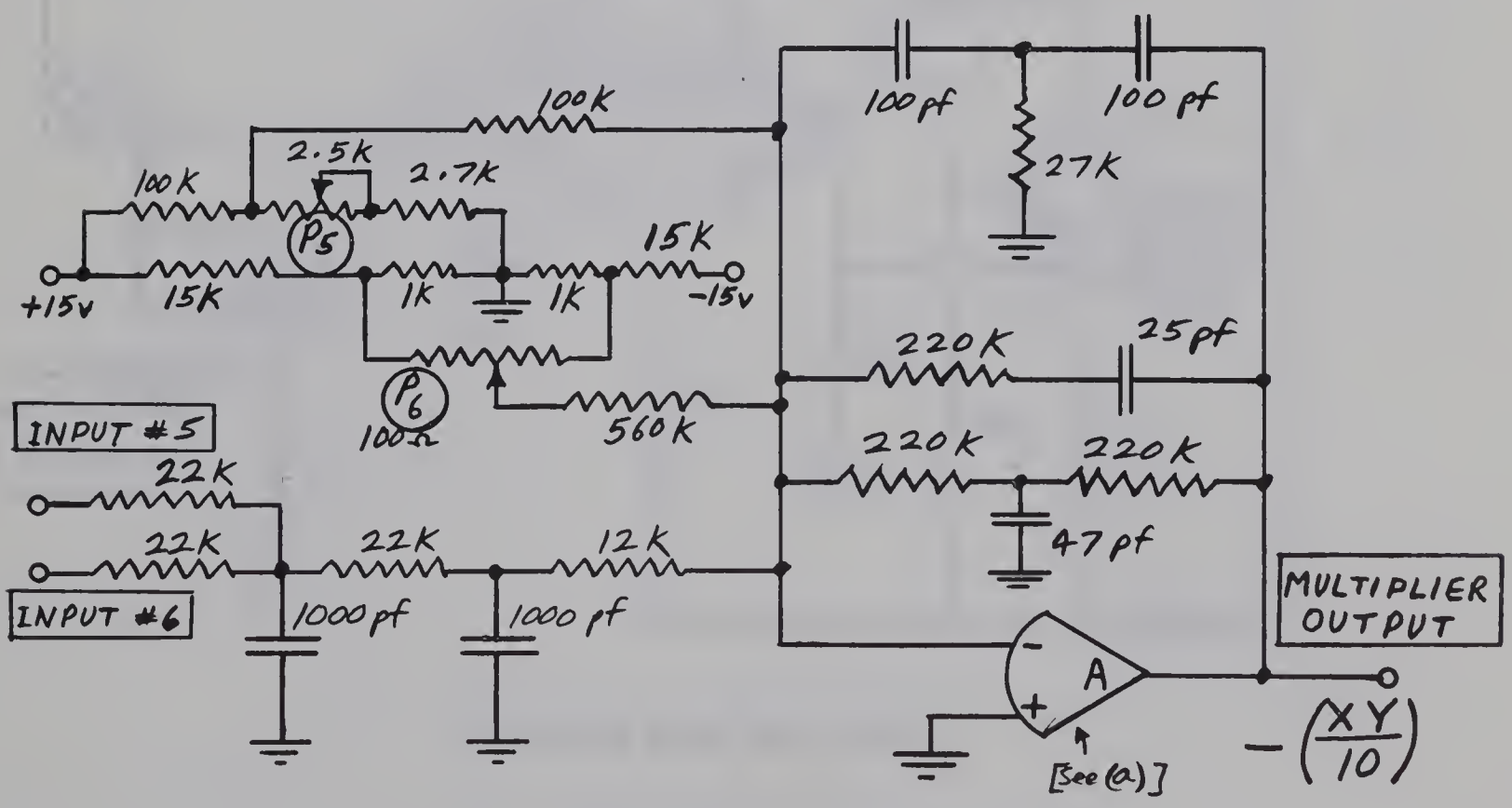


FIG. 5.33 Pulse amplitude modulator (includes bistable flip-flop).



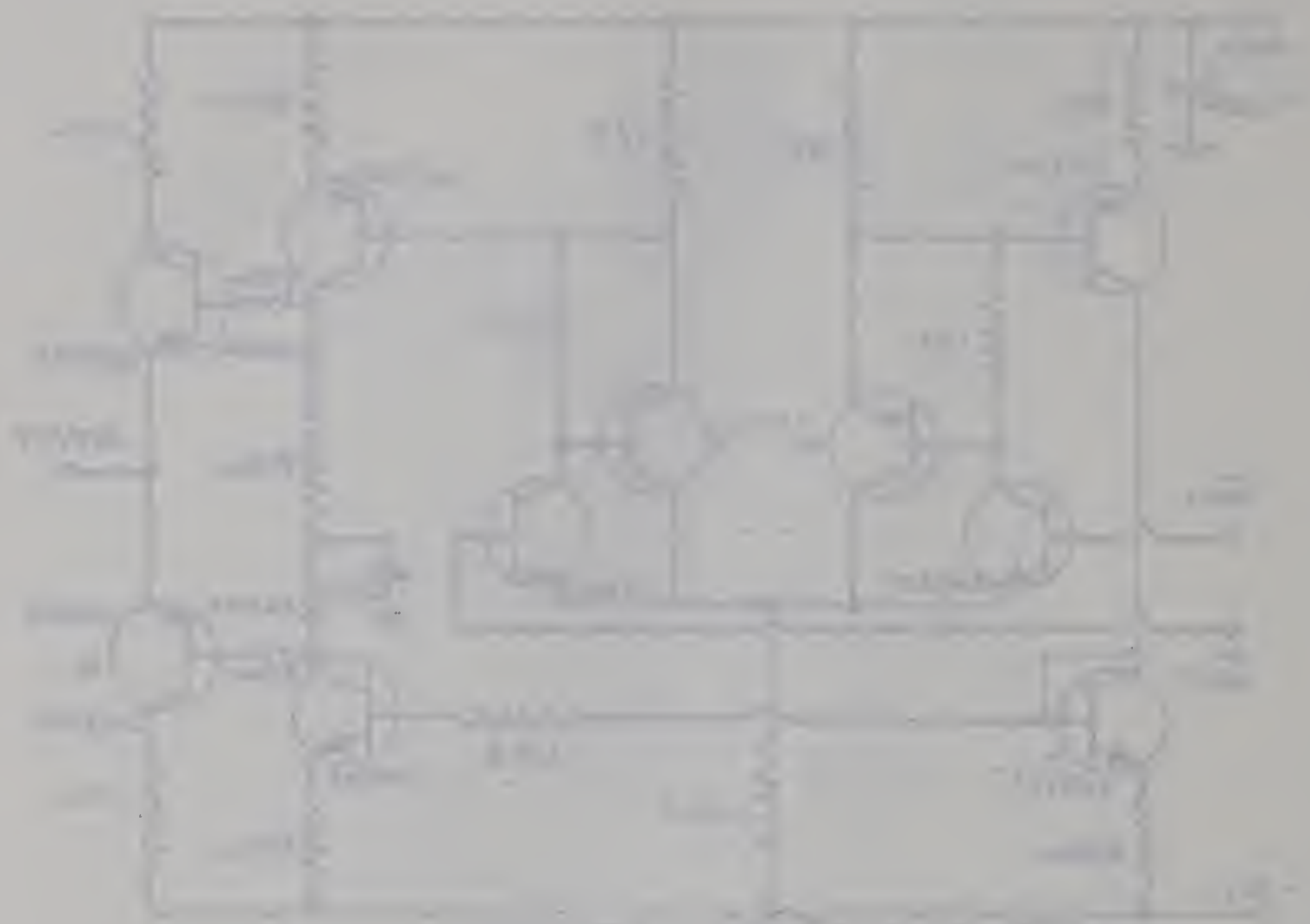


(a) Operational amplifier section.



(b) Filter and bias network section.

FIG. 5.34 Output Butterworth filter-amplifier.



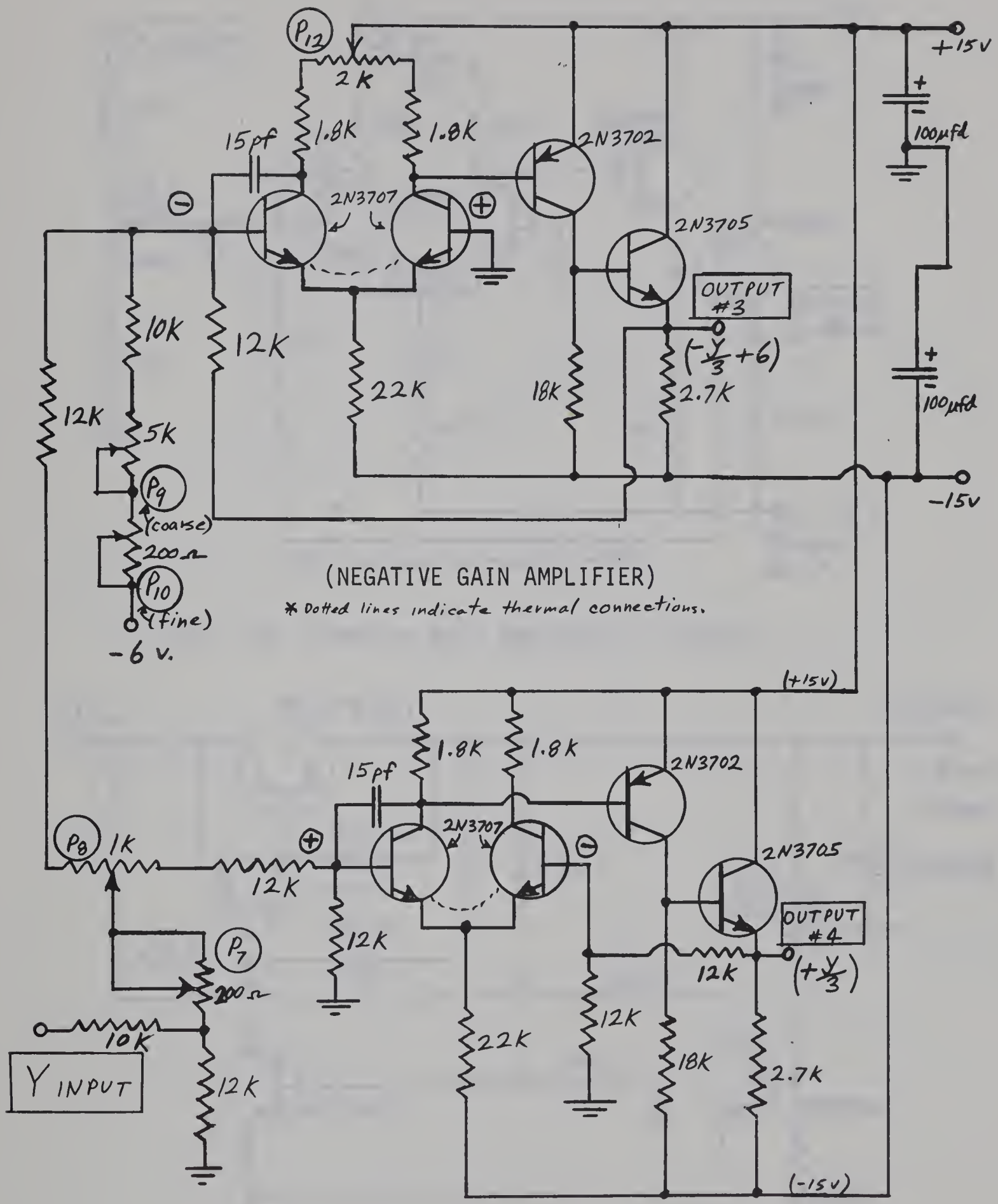


FIG. 5.35 Negative and positive gain input amplifiers (y input).

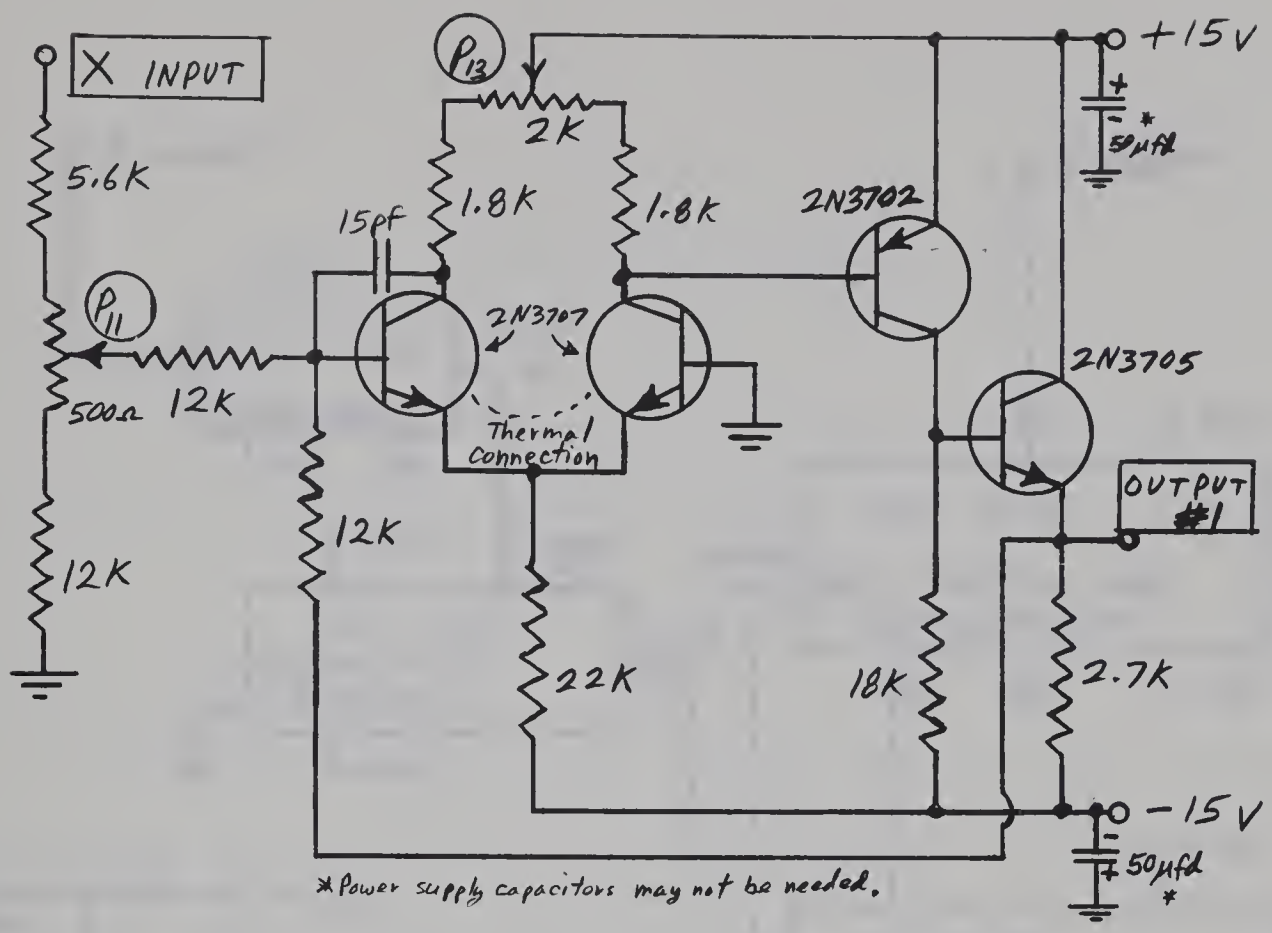


FIG. 5.36 Negative gain amplifier (x input).

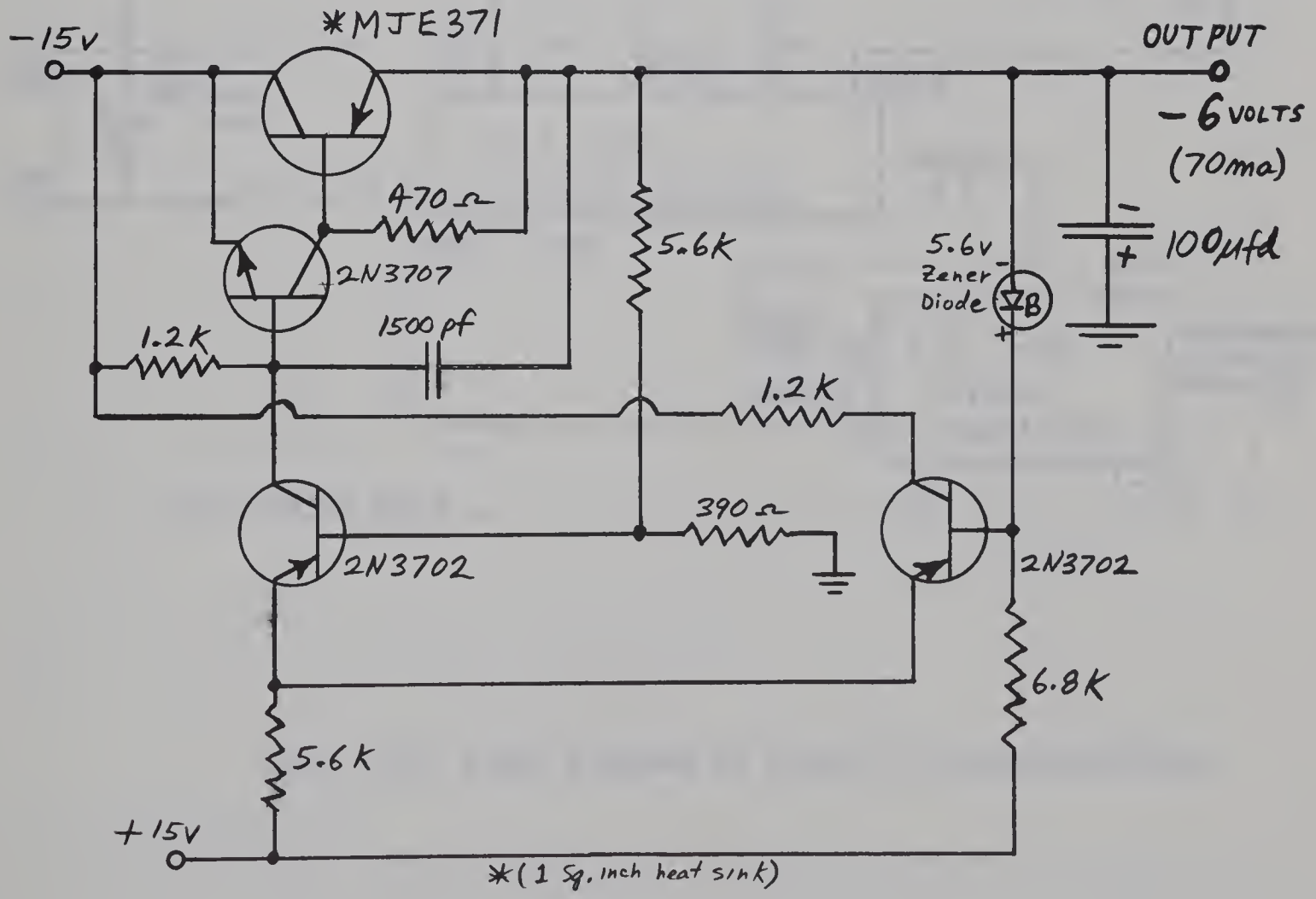


FIG. 5.37 Negative 6 volt power supply.

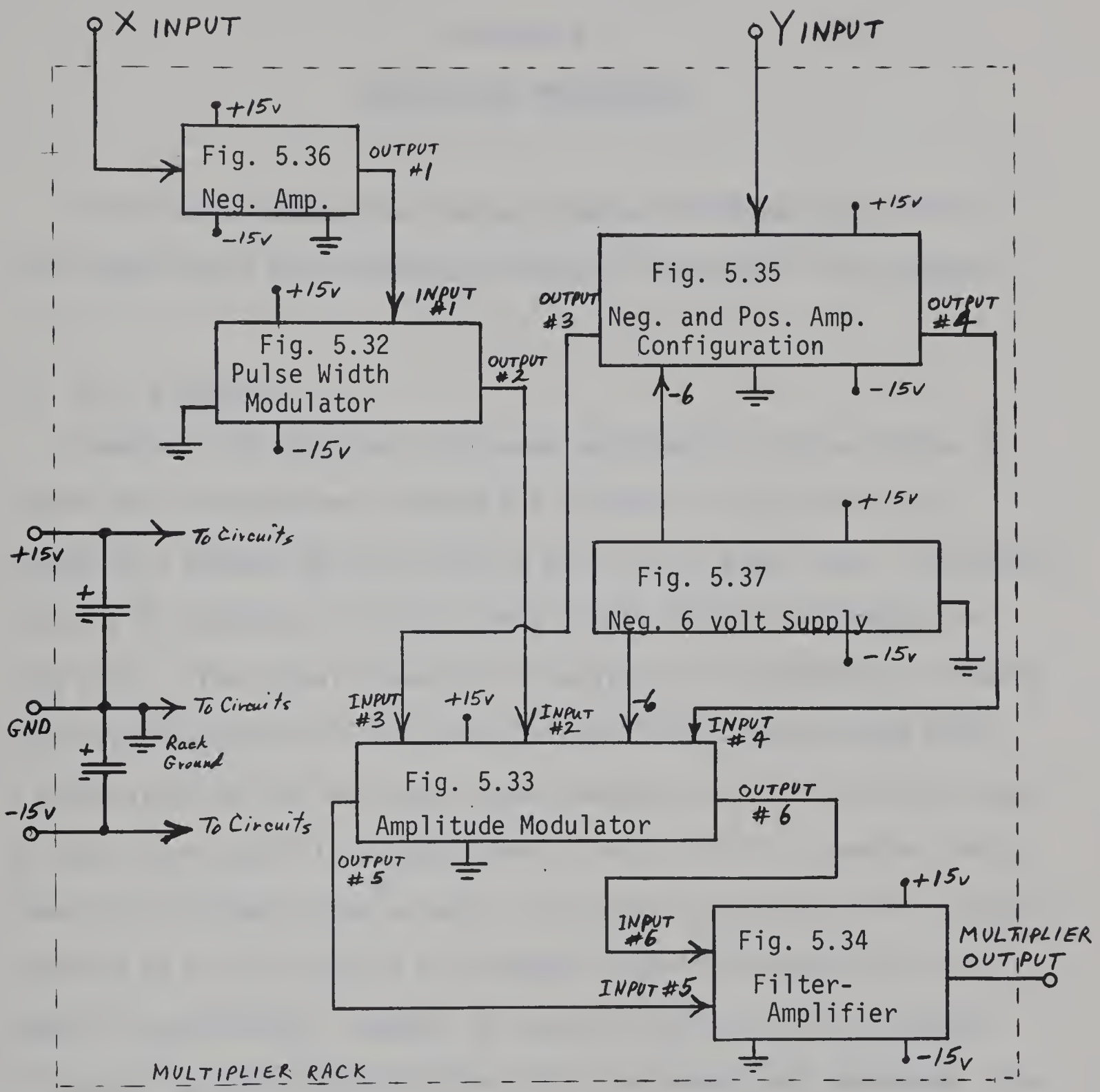


FIG. 5.38 Block diagram of circuit interconnections.

CHAPTER 6

MULTIPLIER PERFORMANCE

This chapter summarizes the performance of the multiplier via brief description and references to tests illustrated in the appendix.

6.1 D.C. Linearity

Numerous four quadrant tests were performed on the multiplier to ensure that the observed accuracy was reliable. The linearity is stated as a maximum deviation from a best fit straight line. The overall accuracy is obtained by forcing the straight line to go through the zero point. The actual linearity of modulation is obtained by allowing the straight line to fit the output without regard to the zero point. A combination of the least mean square method and common sense was used to obtain the best fit straight lines. One of the four quadrant tests (test #3) is shown in the appendix. An overall accuracy of ±0.5 percent referred to a half range 10 volt output (rather than the full 20 volt range) is guaranteed. However, an overall accuracy of ±0.25 percent is typical for the multiplier when it is reasonably well balanced. The linearity of modulation can be guaranteed to be within ±0.25 percent since it is typically about ±0.1 percent.

6.2 D.C. Zero Error

The discrepancy between the overall accuracy and the linearity of modulation mentioned in the previous section is due to the effect of the

zero error of the multiplier. In this context, "zero error" is used to describe the change in output voltage that results when one input is made zero and the other input is varied through its ±10 volt range. This effect occurs due to faulty adding of the waveforms produced by the two choppers. Only slight changes in waveshape cause imperfections in the summation of the two waveforms. The magnitude of the imperfection is represented by these zero error measurements. For x = 0, y = ±10 v, the output remains within ±10 mv of zero (±0.1 percent). For y = 0, x = ±10 v, the output remains within ±3 mv of zero (±0.03 percent). These values are obtained for a well balanced multiplier. If the multiplier drifts out of balance these values will increase. It is not expected that the multiplier will drift out of balance by an amount large enough to cause the error to exceed the guaranteed accuracy. However, periodic checks should be made when the multiplier is initially put to use (about once or twice a month at least) to ensure that the accuracy is maintained.

6.3 D.C. Temperature Drift

There are two locations in the multiplier where the temperature drift is of significant interest. One is the drift at the multiplier output with grounded inputs and the other is the drift of the pulse width modulator. A series of tests indicated that the multiplier output drift was less than or equal to 0.02 percent/^{o}F for a range of +40^{o}F to 110^{o}F (see temperature test #1). This drift is not serious as the output zero adjustment can compensate for this. The drift of the width modulator must be watched more carefully since its drift results in unbalancing of the multiplier. However, when the width

modulator is compensated manually as described in section 5.3(c), the drift can be brought down to 0.01 percent/^{o}F or less for a temperature range of 50^{o}F to 110^{o}F (see temperature test #2). Even when the adjustment is not perfect, drifts less than 0.02 percent/^{o}F can be expected. These measurements assume a warm up period of 5 to 10 minutes. The temperature specifications of the multiplier are suitable for operation in any average room environment which is the type of condition that the multiplier is meant to operate under.

6.4 A.C. Linearity

The A.C. linearity is closely related to the linearity of modulation discussed previously. The distortion of A.C. signals by the multiplier is very low. For y input signals, a maximum distortion of 0.07 percent is observed for a full $\pm$10 volt output. For x input signals, the largest distortion product is less than about 0.04 percent. Measurements were made for frequencies up to 10 KHz and these are shown in test #13. These low distortion figures illustrate the negligible distortion of the operational amplifiers.

6.5 A.C. Zero Error

The term "zero error" is used in the same context here as in section 6.2. This error is the main factor that limits the high frequency performance of the multiplier. At low frequencies, it is no larger than the D.C. zero error, however at higher frequencies it becomes large. It is still acceptable at 5 KHz (0.23 percent for x inputs, and 0.3 percent for y inputs) but it becomes too large at 10 KHz (0.44 percent for x inputs, and 0.57 percent for y inputs). See

test #14 for the complete results.

The cause of the error is imperfect summation at high frequencies due to waveshape imperfections and due to phase shift differences that begin to occur between the two channels. There is a possibility of improving the high frequency performance by adjusting the phase shifts of the two chopping channels with trimming capacitors. However attempts to do this proved to be quite difficult and any improvement obtained required numerous trial and error settings of the capacitors since the balance of the multiplier had to be readjusted for every capacitor adjustment. Thus the decision was made to not attempt to improve the operation of the multiplier past the 5 KHz frequency response originally desired.

6.6 A.C. Modulation Distortion

With the filter design finally chosen (f_c = 15 KHz), the possible distortion due to frequencies up to 15 KHz was only in the order of 0.1 percent (this being mainly due to the 200 KHz pulse frequency). With the operation of the multiplier limited to 5 KHz, the modulation distortion was considered negligible.

6.7 A.C. Phase Shift

Investigation of the phase shift of the complete multiplier showed that the phase shift was due to the filter only. The measured phase shift (shown in test #15) was only 8^o at 1 KHz and did not exceed 39^o at 5 KHz.

6.8 Power Supply Dependence

To test the dependence of the output voltage on the power supply voltages, each supply was increased and decreased by 0.5 volts. The results are shown in Fig. 6.1. (Note: the column + 0.5 v in the figure denotes increasing the magnitude of the supply voltage, eg. -15.5.)

Supply Changed	+ 0.5 v	- 0.5 v
+ 15 volt supply	+ 0.15%	- 0.5 %
- 15 volt supply	- 0.2 %	+ 0.5 %
- 7 volt supply	- 0.25%	+ 0.5 %

FIG. 6.1 Output voltage dependence on supply voltages.

6.9 Summary of Guaranteed Specifications

The specifications given below are considered reliable for any multiplier that might be built from the circuits contained in this thesis. In most cases they will be better than those stated but are not guaranteed to be so.

D.C. Linearity ..... $\leq \pm$ 0.5 % (referred to 10 volts),

A.C. Linearity ..... $\leq$ 0.1 % distortion (up to 5 KHz),

A.C. Distortion..... $\leq$ 0.5 % distortion (up to 5 KHz),

D.C. Zero Error..... $\leq$ 0.1 % ,

A.C. Zero Error..... $\leq$ 0.5 % (up to 5 KHz),

D.C. Temp. Drift.... $\leq$ 0.025%/^{o}F (for grounded inputs),

A.C. Phase Shift.... $\leq$ 40^{o} (up to 5 KHz),

A.C. Frequency Limit..... $(f_x + f_y) \leq$ 5 KHz,

Input Impedance (x input)..... $\geq$ 10 K ohms,

Input Impedance (y input)..... $\geq$ 10 K ohms.

CHAPTER 7

CONCLUSIONS

The performance obtained from the completed multiplier proved to be satisfactory in every respect. Some of the parameters such as D.C. modulation linearity and A.C. linearity are much better than needed to meet the original requirements.

The amount of phase shift introduced by the filter can be controlled to some extent by altering its cutoff frequency. If desired, the multiplier can be constructed to accommodate interchangeable amplifier-filter printed circuit boards to allow some control of the multiplier characteristics. A higher cutoff frequency would reduce the phase shift for higher output frequencies if the increase in pulse frequency distortion was tolerable. If an especially low pulse frequency distortion is required, the cutoff frequency can be lowered at the expense of increased phase shift.

The temperature drift of the output amplifier could possibly be improved by the use of dual transistors for the input stages. Another possibility is the use of an integrated circuit amplifier to replace the input stages.

The general performance of the multiplier would be improved if a faster and more precise chopper could be developed in the future.

However, for the present, the multiplier described in this thesis gives good performance for a relatively low cost.

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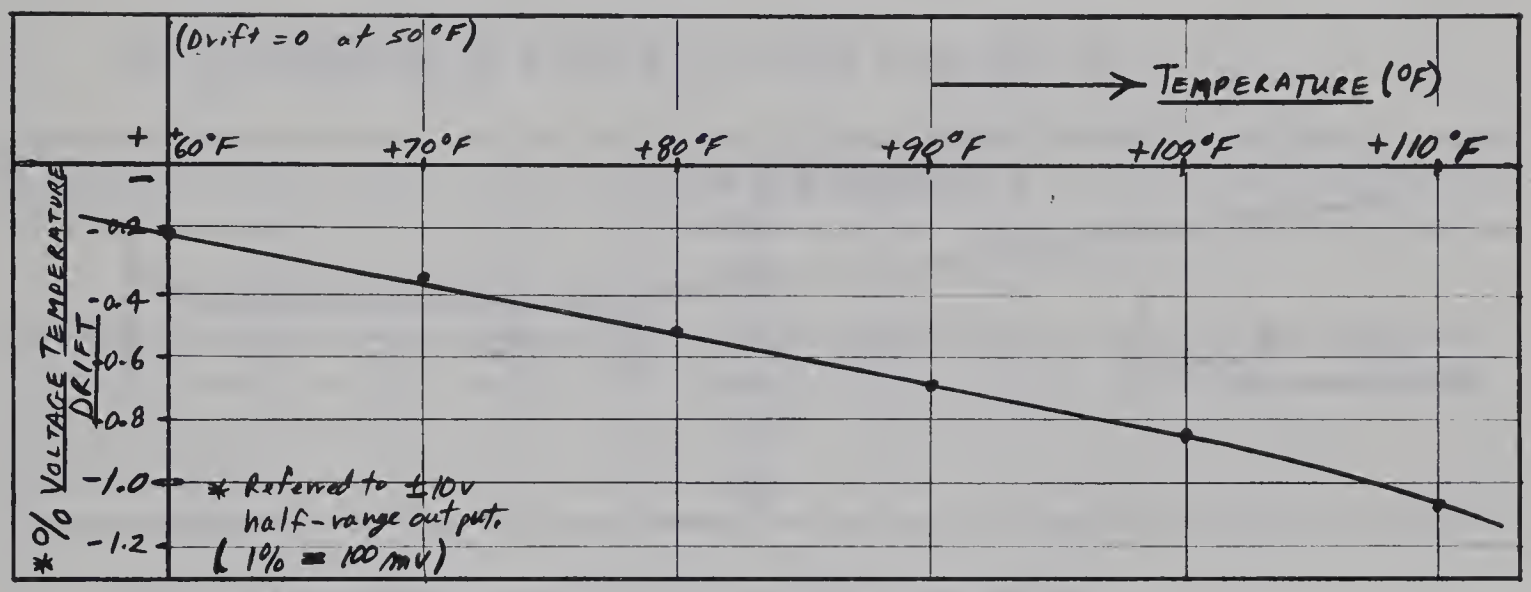
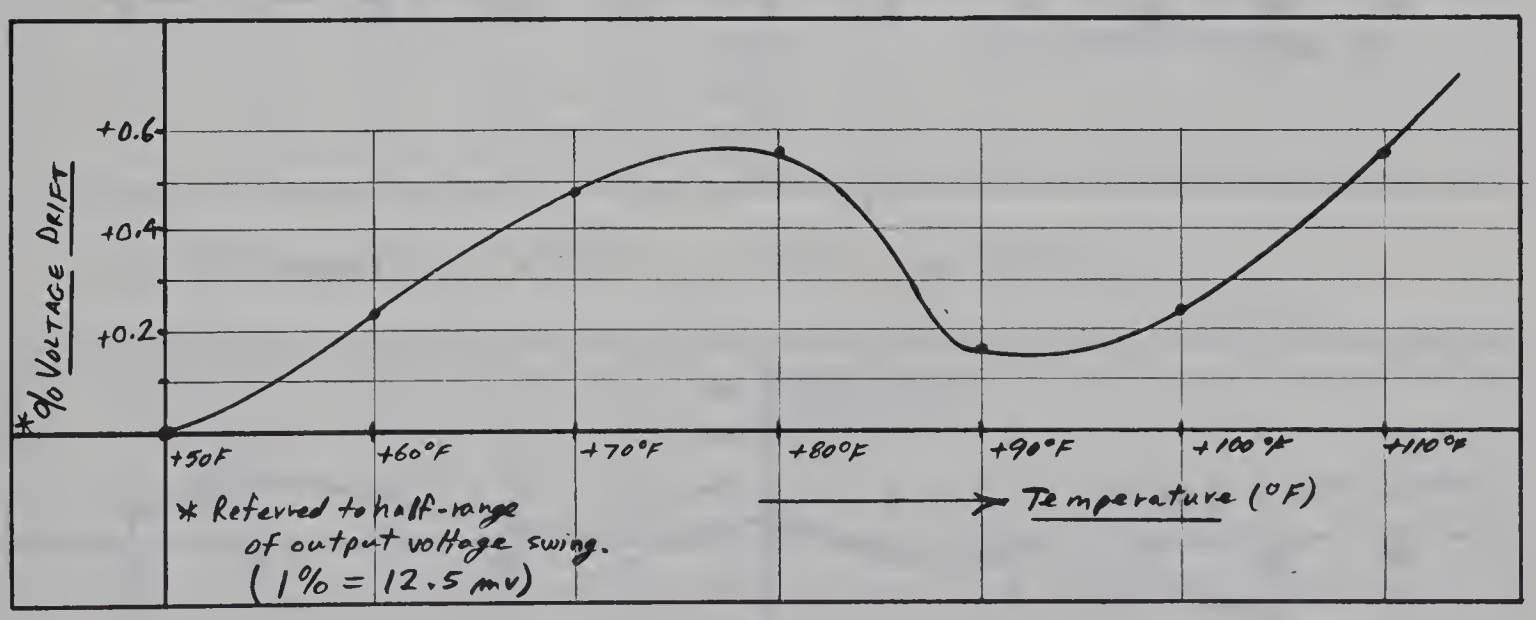
APPENDIX A

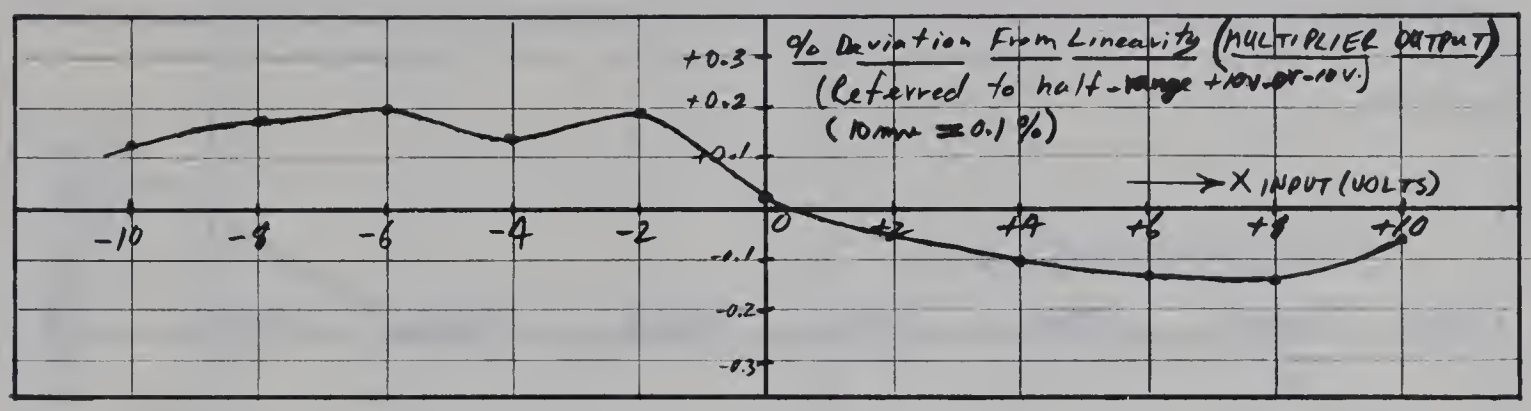
MULTIPLIER PERFORMANCE TESTS



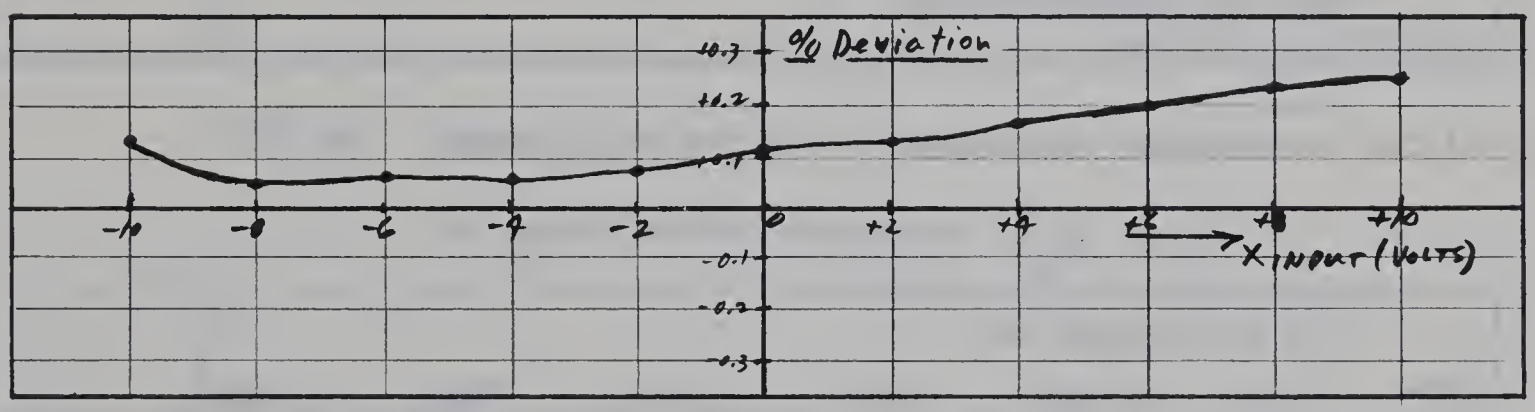
TEST #1. Multiplier output temperature drift.



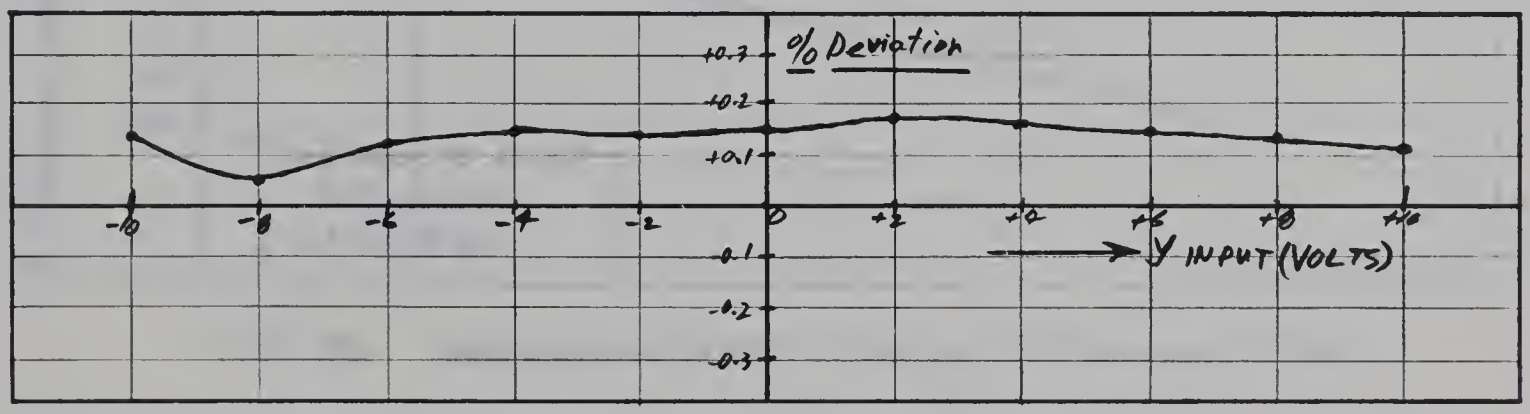
TEST #2. Pulse width modulator temperature drift (complete modulator put in oven).



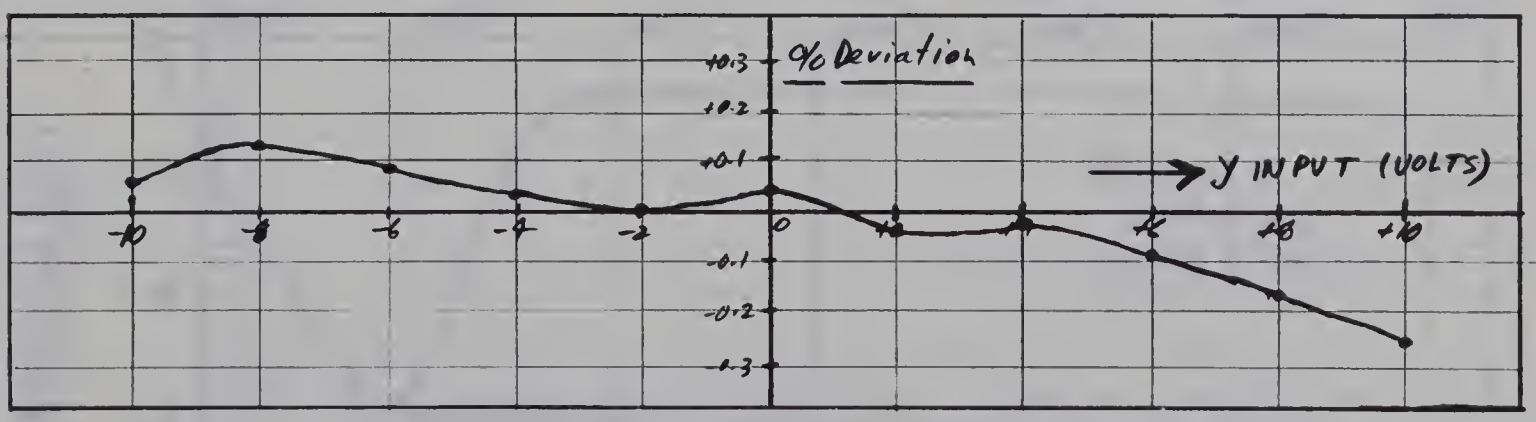
(a) X Linearity (y = +10 v, x = -10 v to +10 v).



(b) X Linearity (y = -10 v, x = -10 v to +10 v).

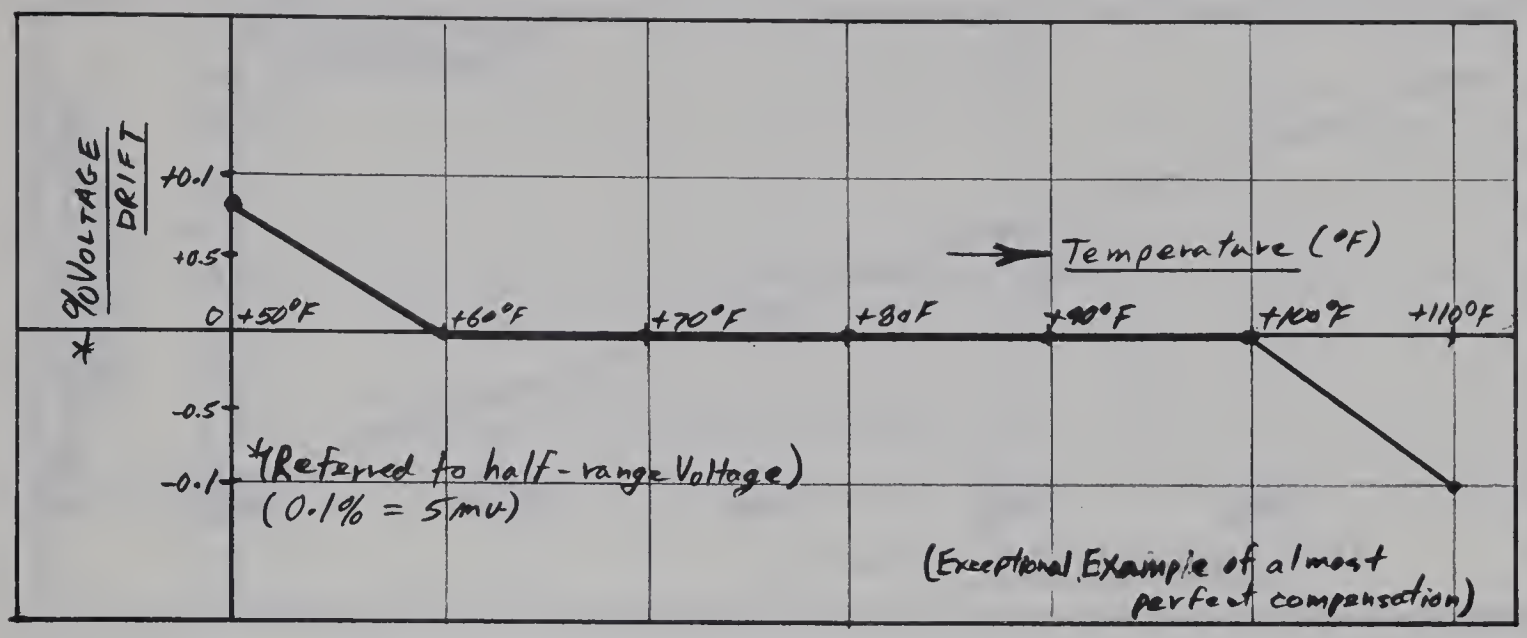


(c) Y Linearity (x = -10 v, y = -10 v to +10 v).

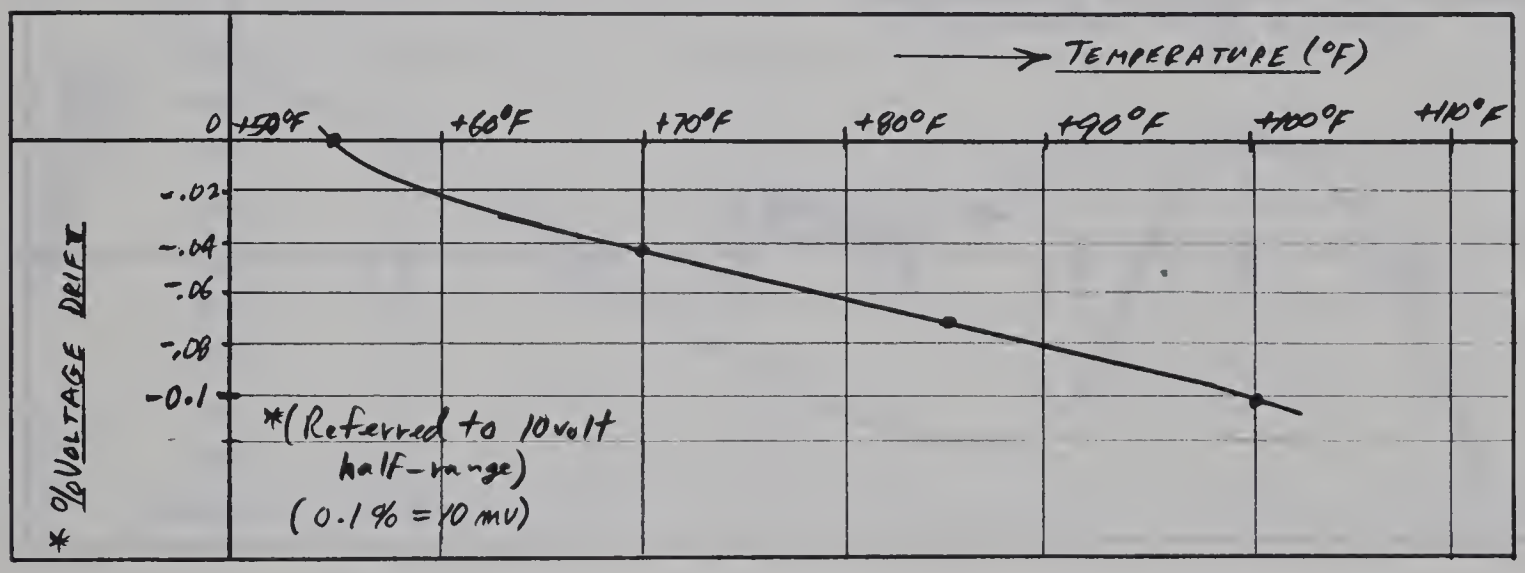


(d) Y Linearity (x = +10 v, y = -10 v to +10 v).

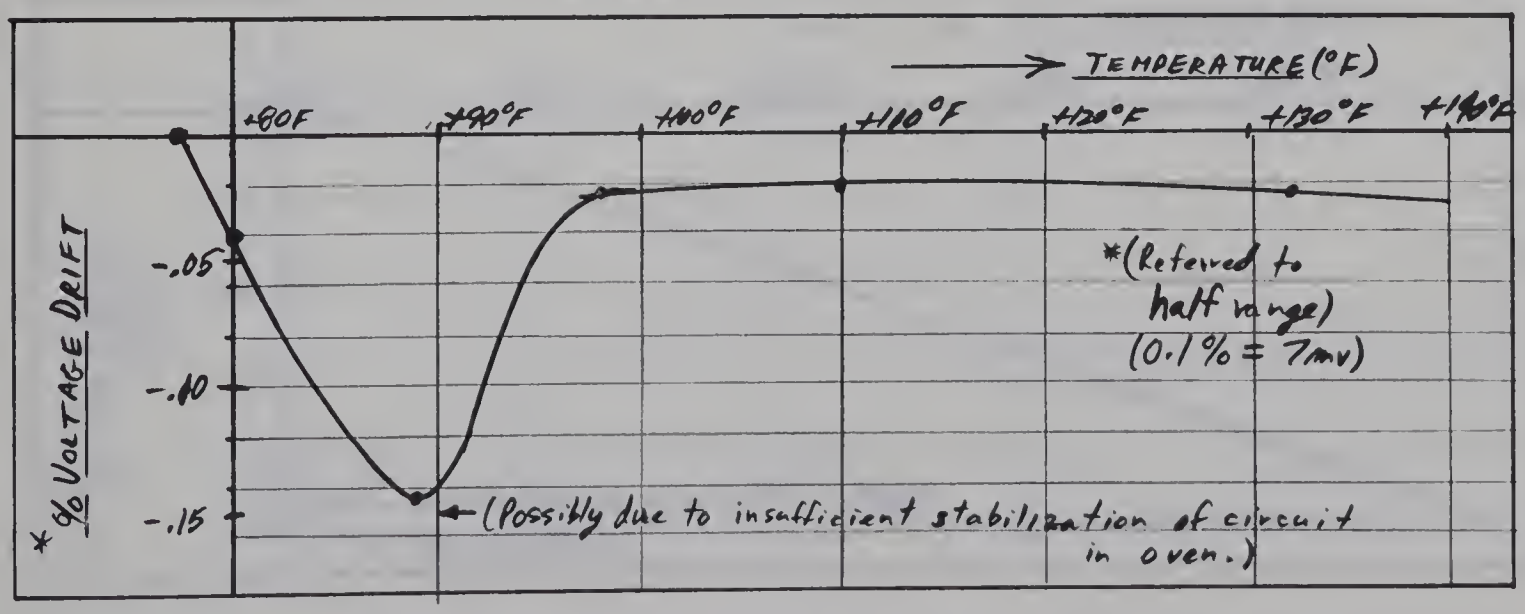
TEST #3. Four quadrant D.C. linearity test. (Typical Test)



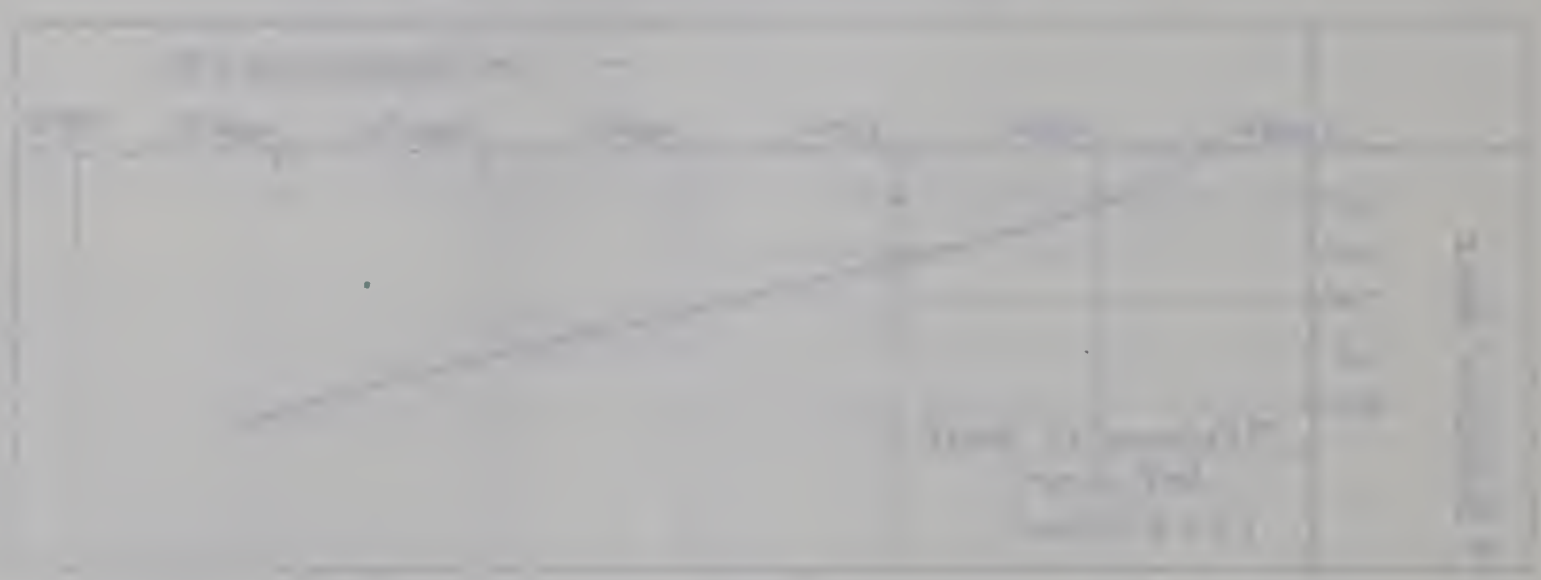
TEST #4. Temperature drift of compensated comparator section of pulse width modulator. (Fig. 5.11)

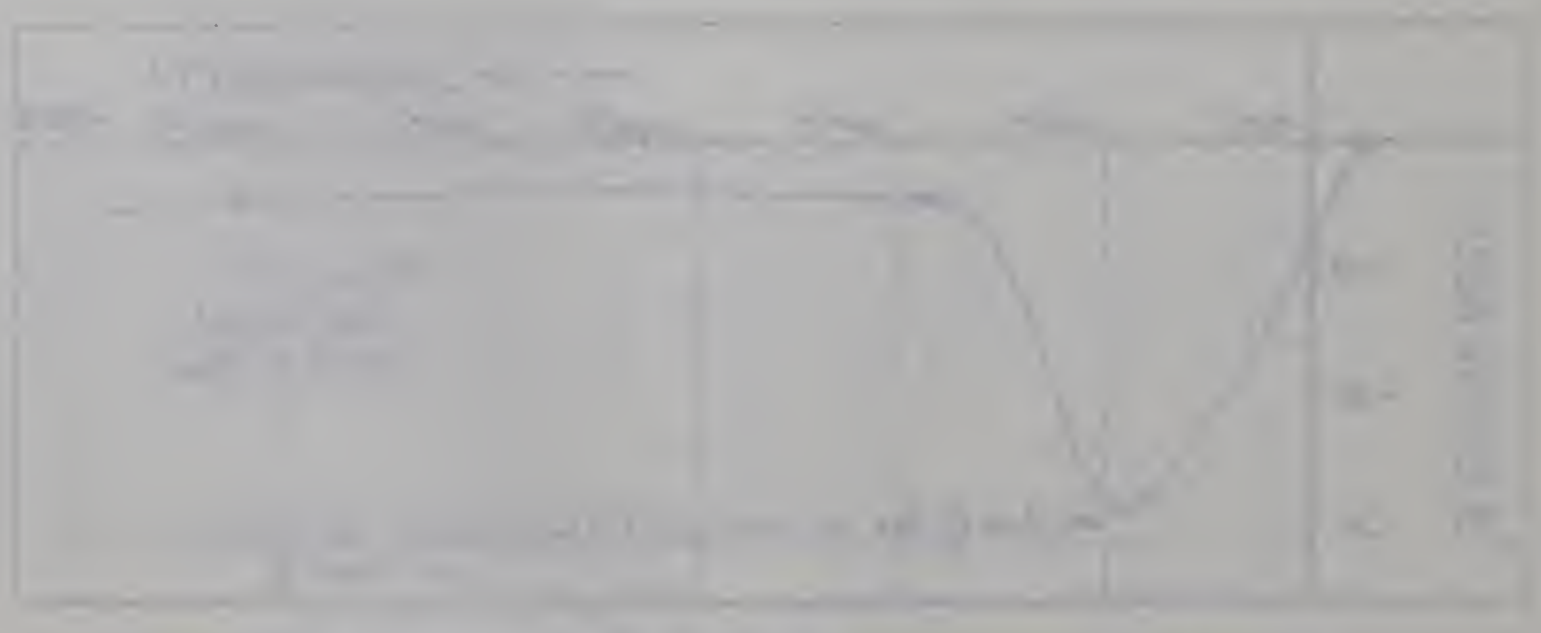


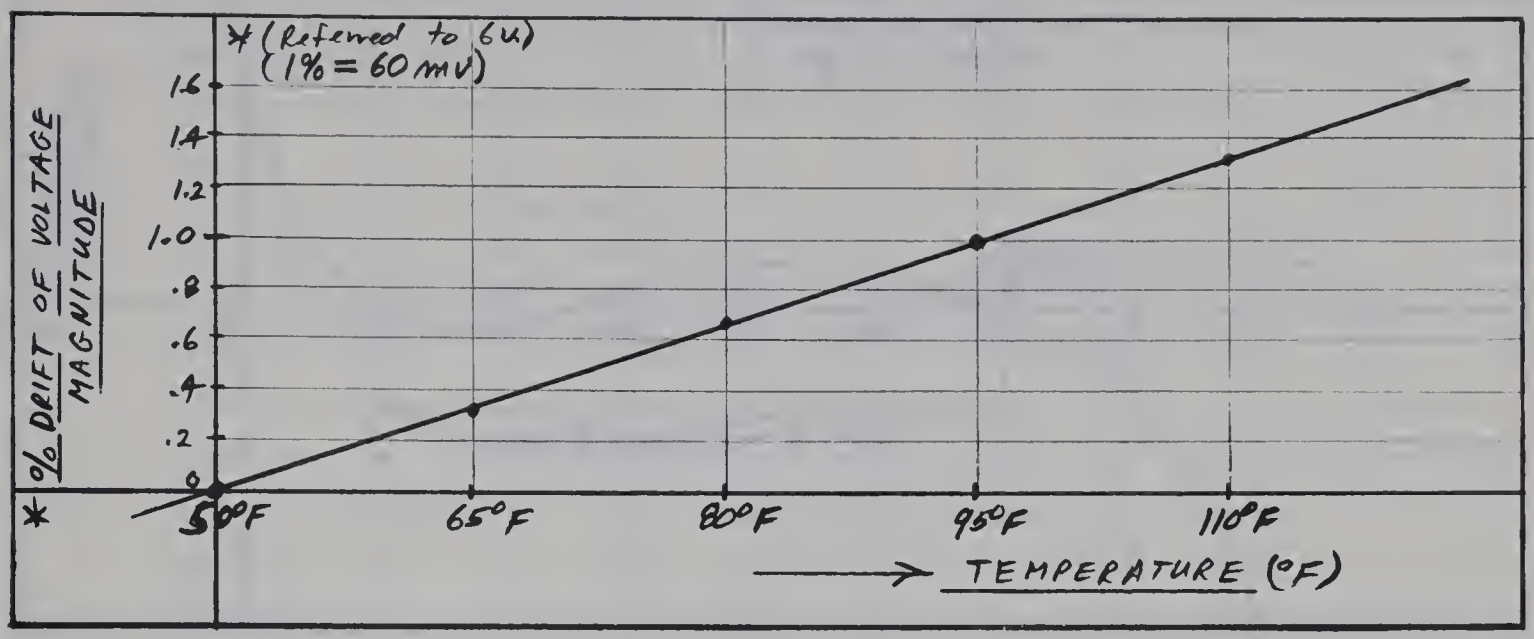
TEST #5. Temperature drift of output filter-amplifier.



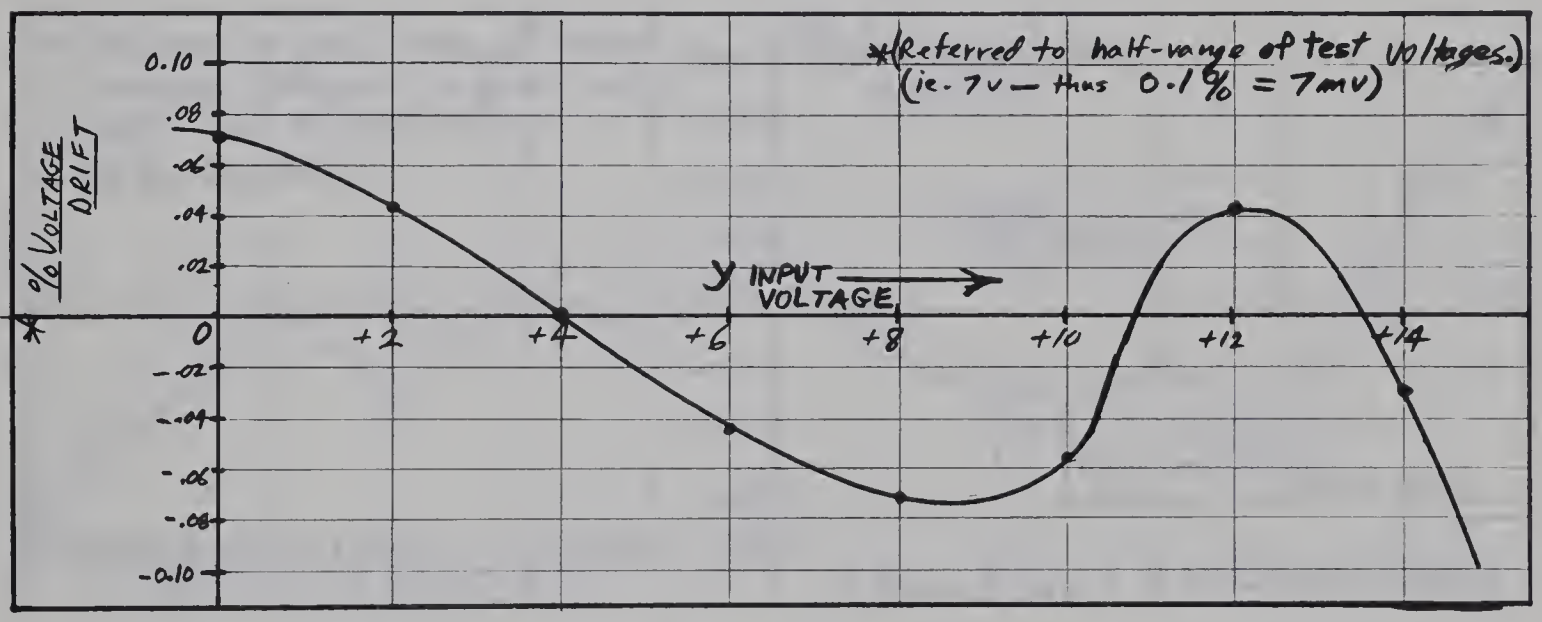
TEST #6. Temperature drift of typical input amplifier.



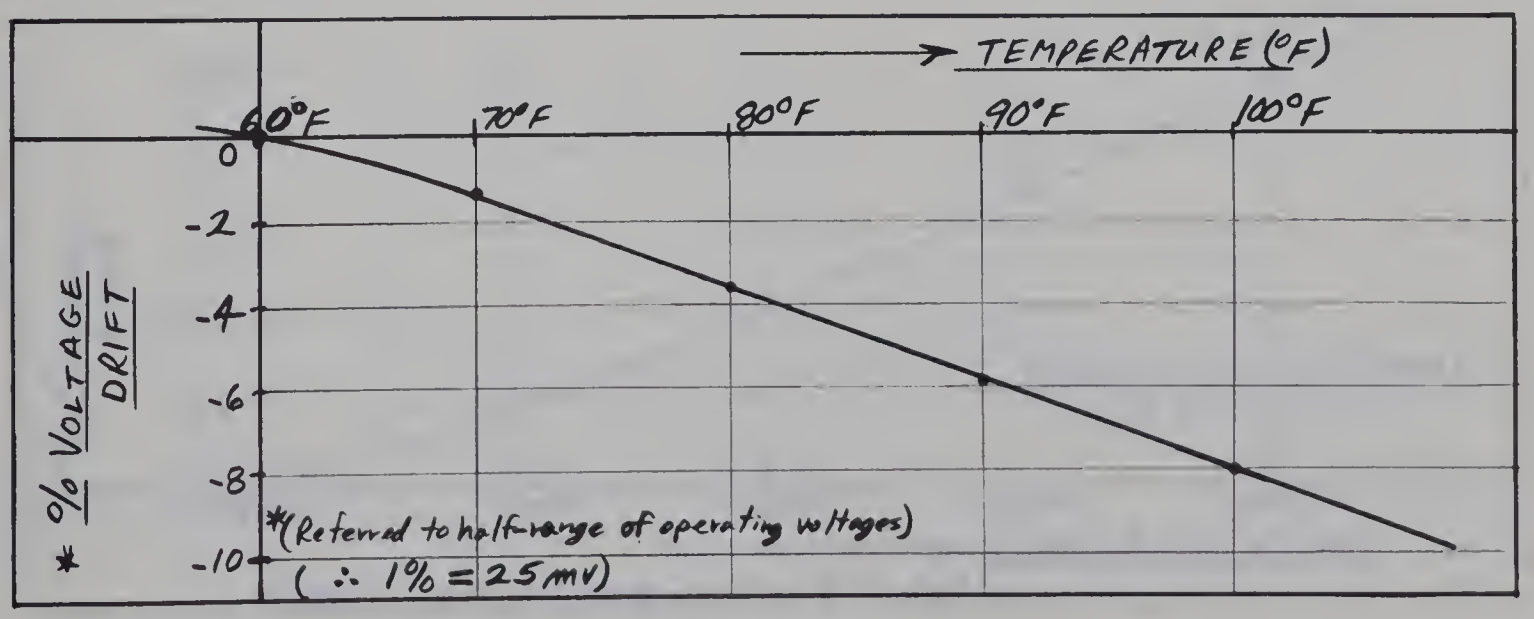




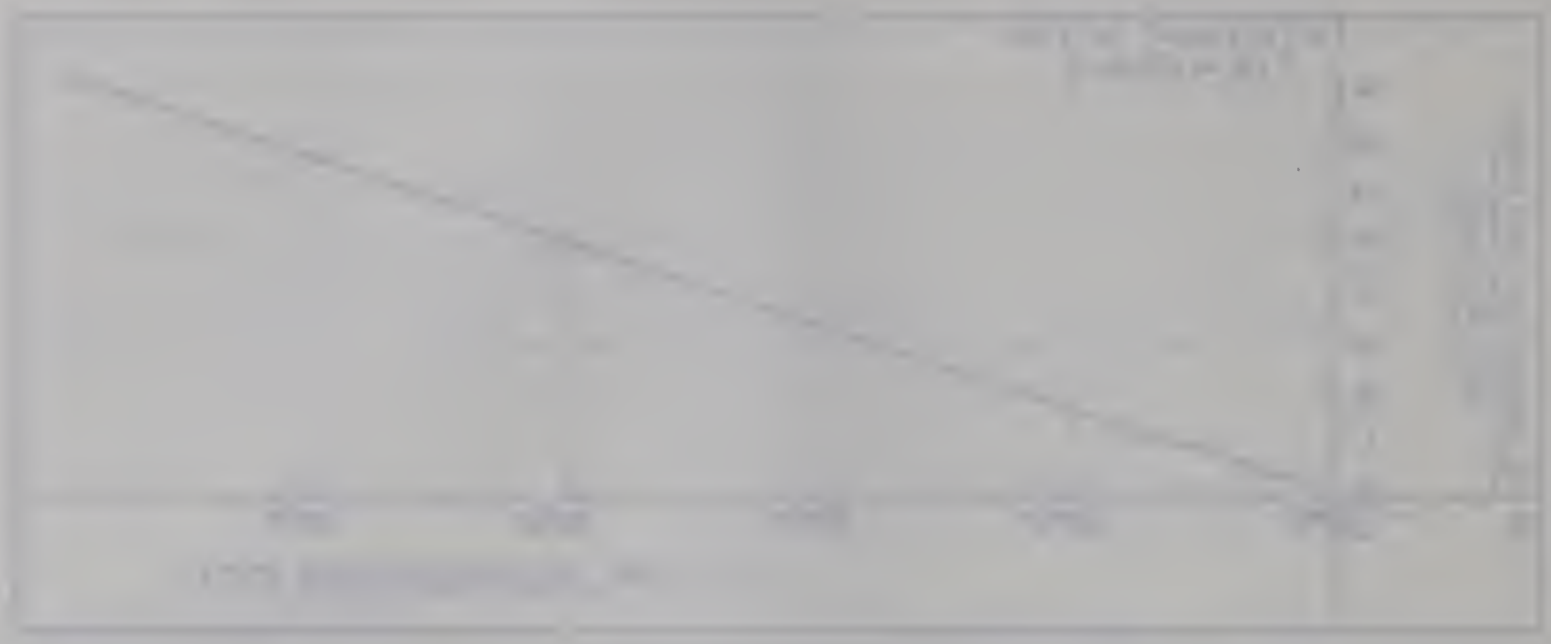
TEST #7. Temperature drift of negative 6 volt supply.

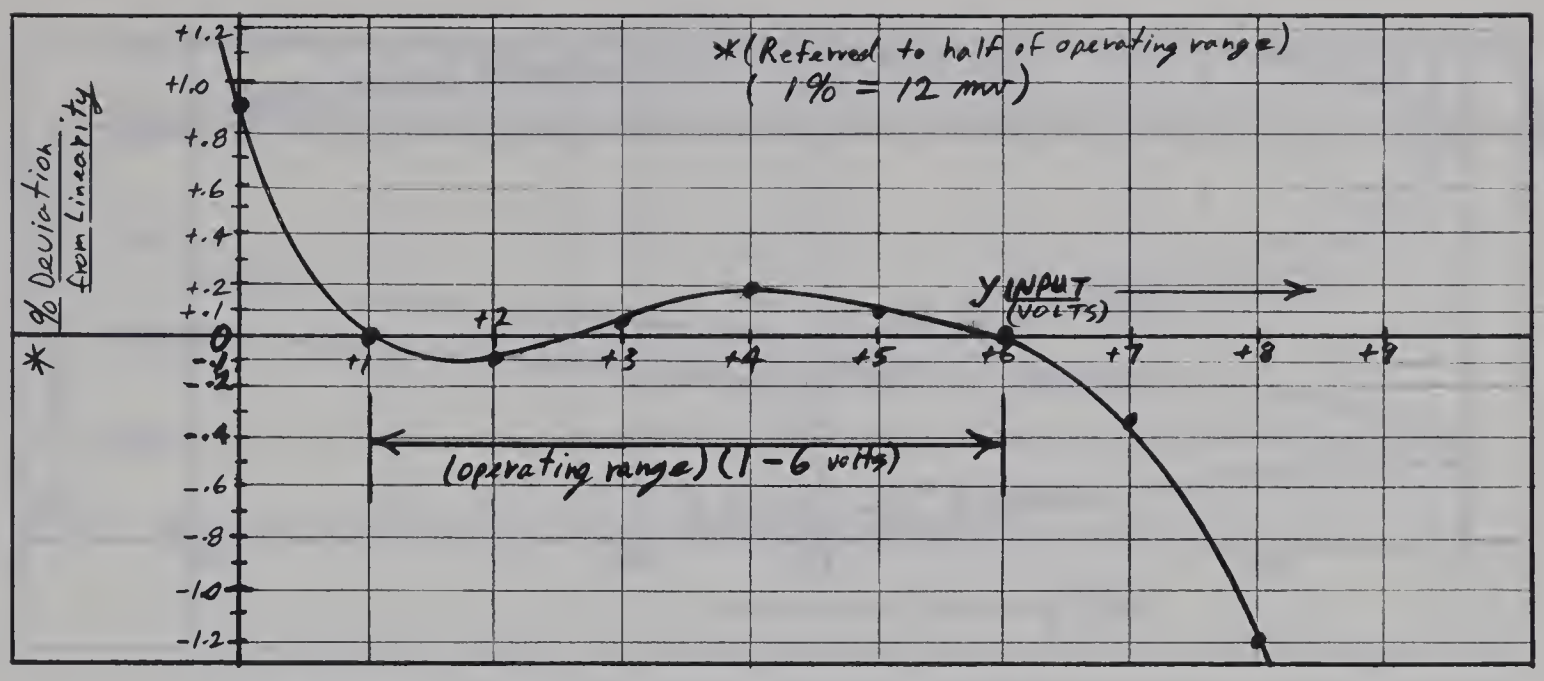


TEST #8. Linearity of tunnel diode hybrid chopper. (Fig. 5.20)

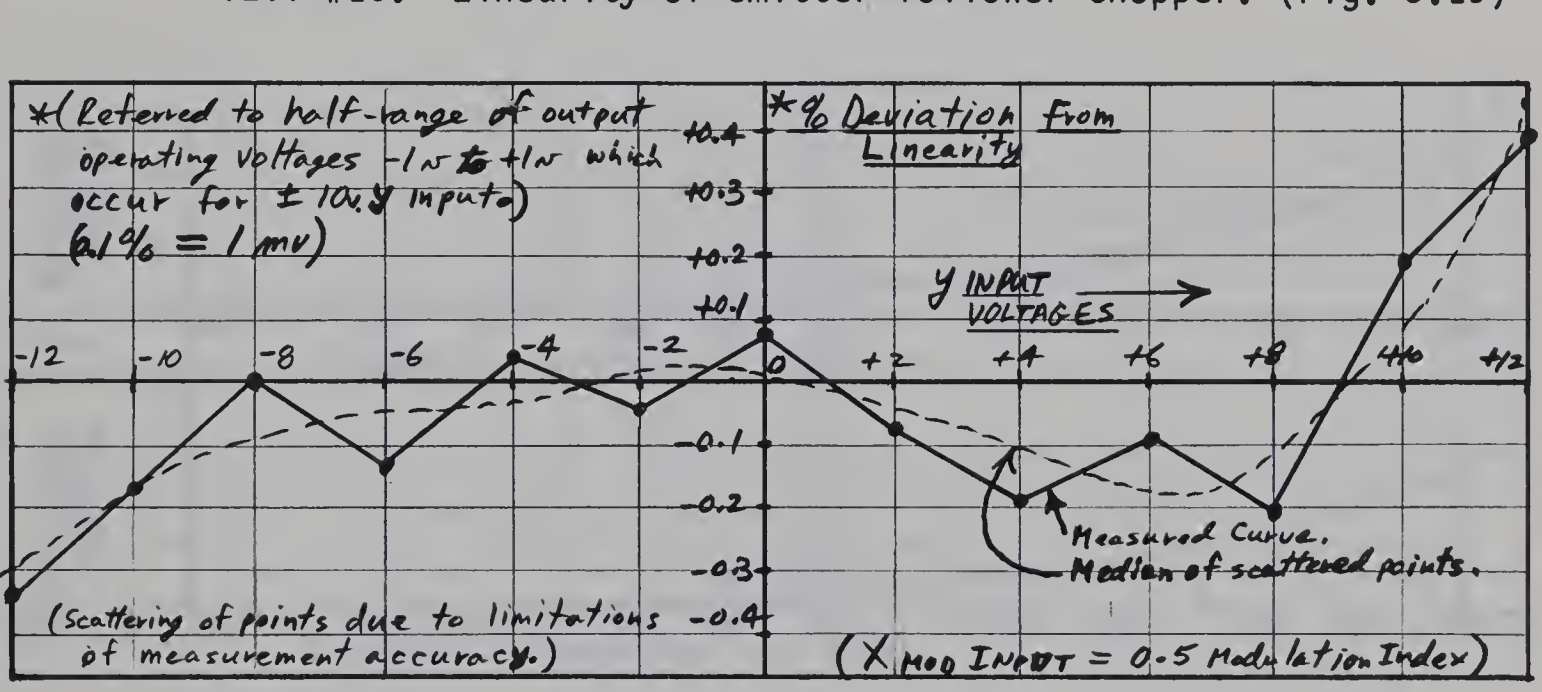


TEST #9. Temperature drift of typical hybrid chopper.

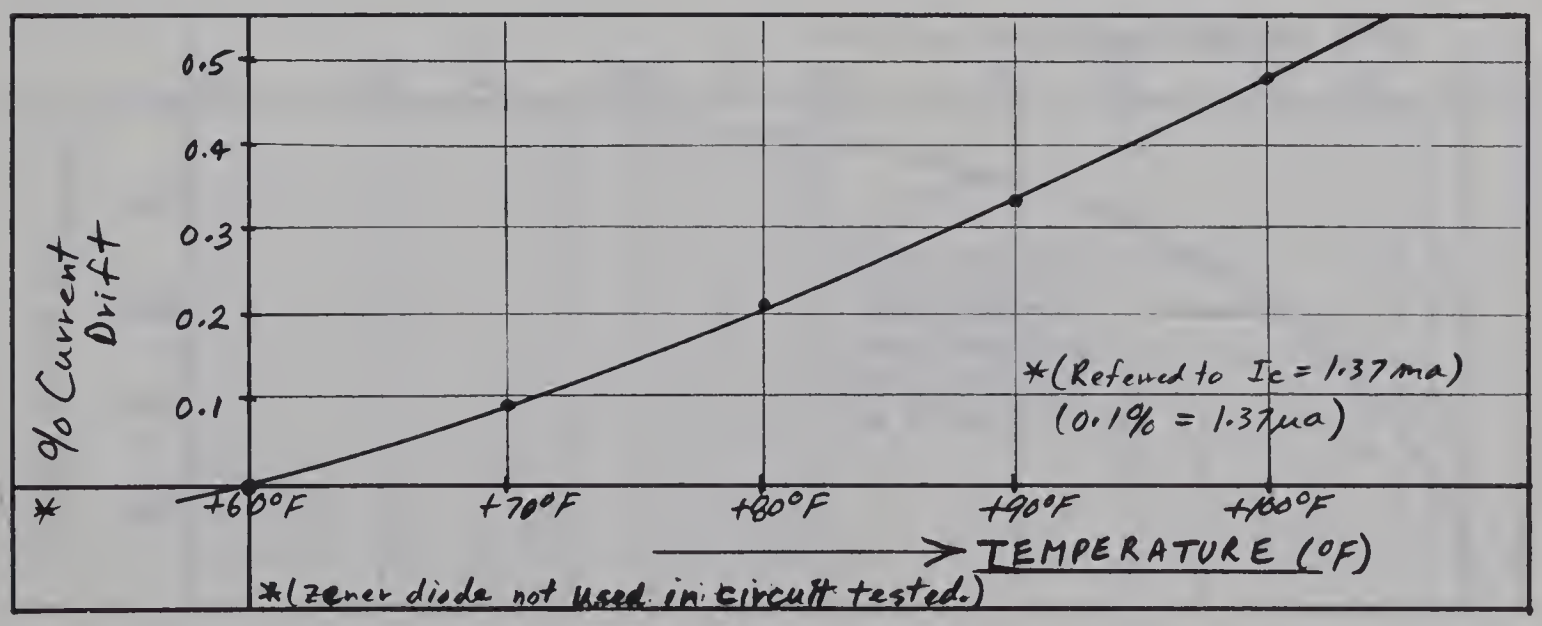




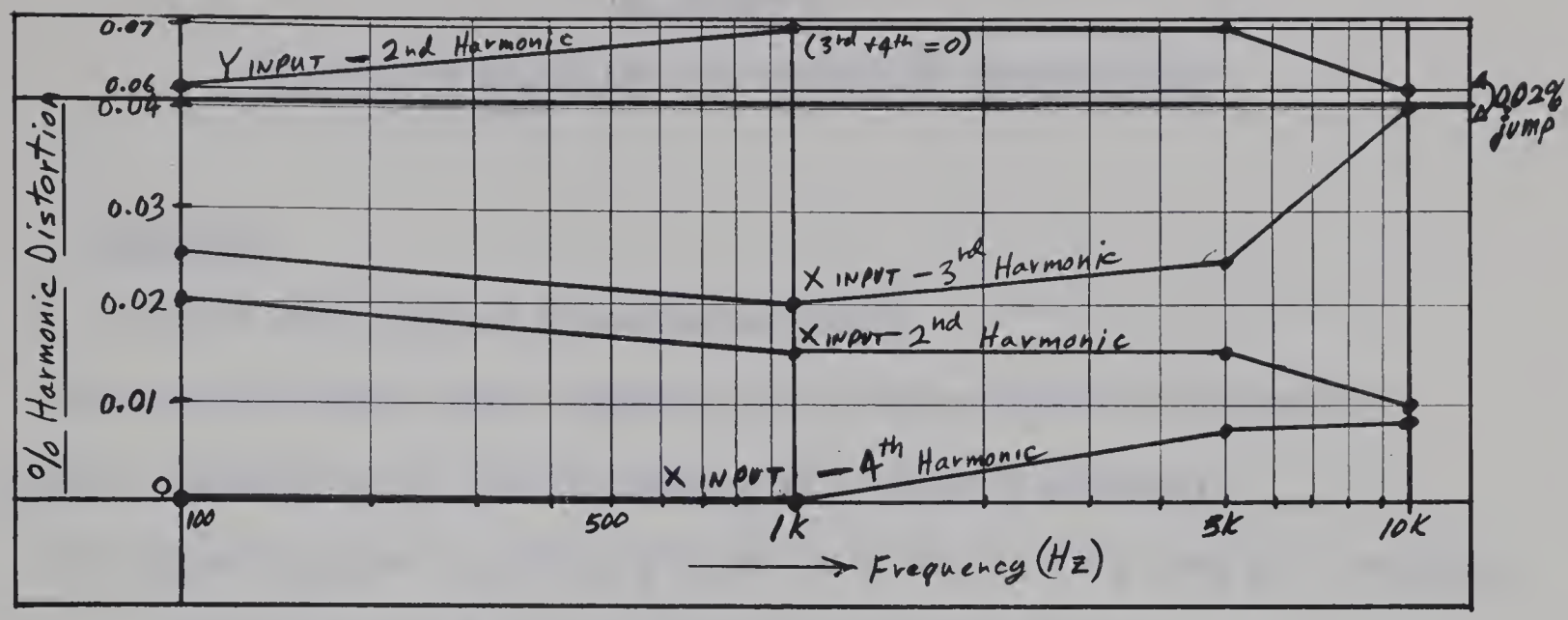
TEST #10. Linearity of emitter follower chopper. (Fig. 5.19)



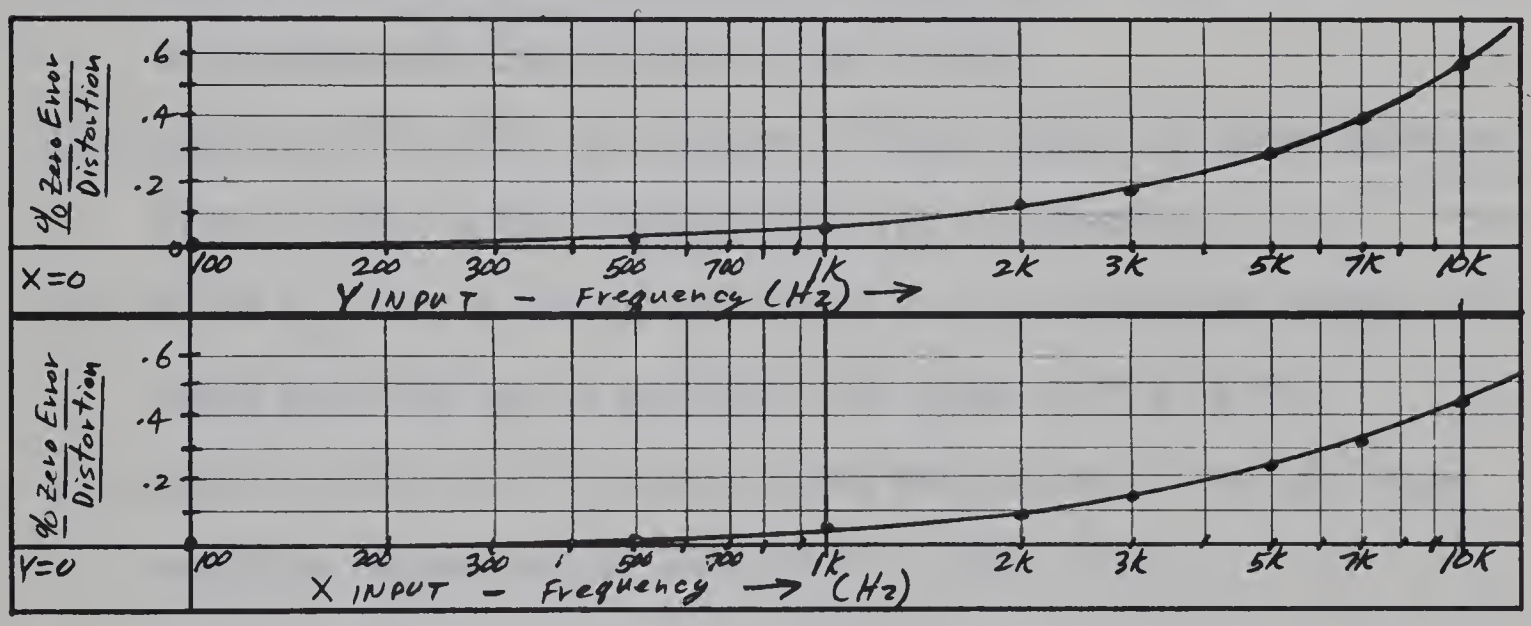
TEST #11. Linearity of amplitude modulator. (Fig. 5.22)



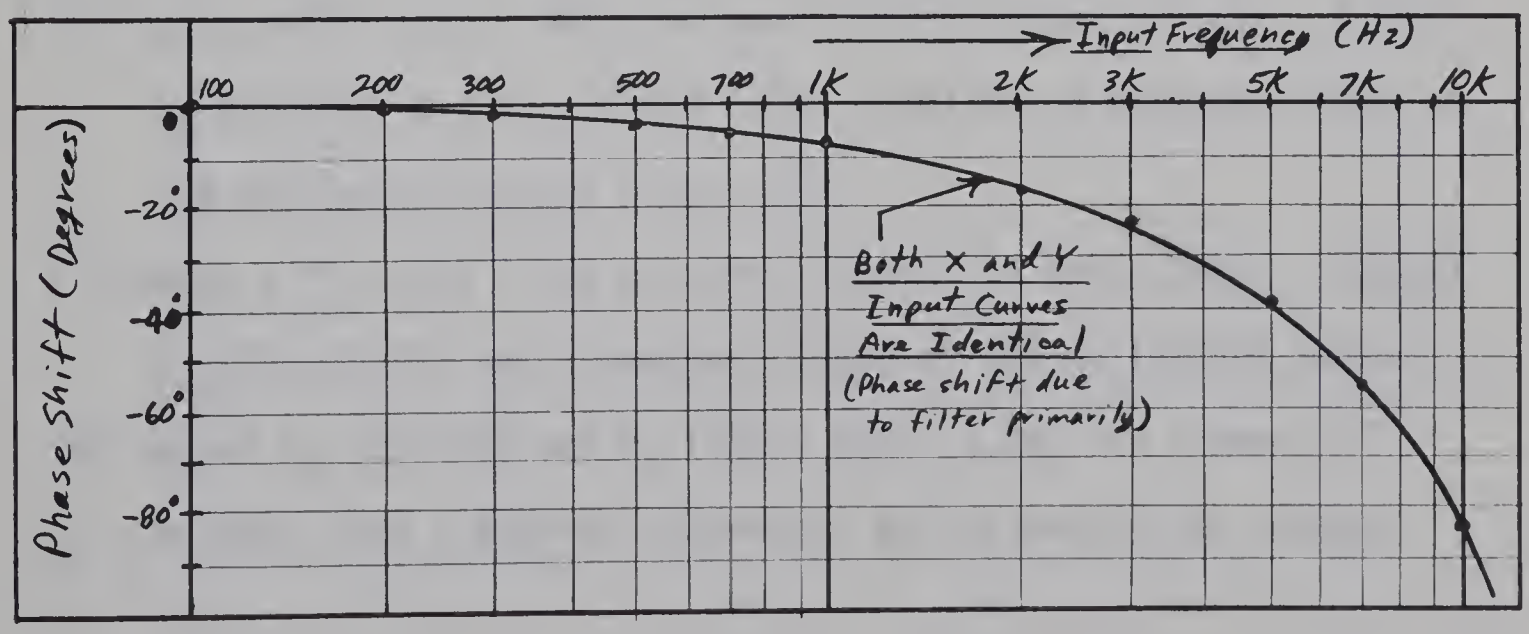
TEST #12. Temperature drift of compensated current source.



TEST #13. A.C. linearity VS frequency.



TEST #14. A.C. zero error VS frequency.



TEST #15. A.C. phase shift VS frequency.

APPENDIX B

MULTIPLIER BALANCING AND OPERATING INSTRUCTIONS

I. BALANCING

A. Initial Setup Before Accurate Balancing

Turn on multiplier power supplies and allow multiplier to warm up before proceding with the following steps (about 5 minutes).

(1) Adjust P_{12} and P_{13} (Fig.'s 5.35 and 5.36) until a zero D.C. voltage results at the Y input and X input, respectively.

(2) Adjust P_1 (Fig. 5.32) to produce a sweep waveform period of 5 microseconds (Test Point 1, Fig. 5.32).

(3) Adjust P_2 (Fig.5.32) to produce a linear appearing sweep waveform (T.P. 1, Fig. 5.32). Repeat step (2) if necessary.

(4) Adjust P_4 (Fig. 5.32) to the center of its adjustable range. Leave shorting bar in position 1 as shown in Fig. 5.32.

(5) Adjust P_3 (Fig. 5.32) to give a 50% duty cycle to the amplitude modulator output pulse train (T.P. 2, Fig. 5.33).

B. Accurate Balancing of the Multiplier

(6) Apply a $\pm$10 volt 1 KHz sine wave signal to the x input. Adjust P_9 (coarse) and P_{10} (fine) (Fig. 5.35) for a minimum signal at the multiplier output (Fig. 5.34).

(7) Apply a $\pm$10 volt 1 KHz sine wave signal to the y input. Adjust P_8 (Fig. 5.35) for a minimum signal at the multiplier output.

(8) Adjust P_5 (coarse) and P_6 (fine) (Fig. 5.34) for a zero D.C. voltage (use a digital voltmeter) at the multiplier output.

Remove all inputs before adjusting for a zero voltage.

C. X Linearity Adjustment

(9) Apply a +10 volt D.C. signal to the y input. Also apply a ±10 volt 1 KHz sine wave signal to the x input. Connect the multiplier output to a wave analyzer (preferably a Hewlett Packard Model 302A) or to a distortion analyzer. Then adjust P_2 (Fig. 5.32) for a minimum value of 2nd harmonic (or a minimum overall distortion if using a distortion analyzer).

II. TEMPERATURE COMPENSATING THE WIDTH MODULATOR

(10) Put complete multiplier in a temperature controlled testing oven. Use a digital voltmeter (D.V.M.) to measure the voltage at T.P. 3 (Fig. 5.33). Potentiometer P_4 (Fig. 5.32) is used to compensate the temperature drift. Because changing P_4 will change the duty cycle of the pulse train at T.P. 2 (Fig. 5.33), the D.V.M. reading will change also. This effect is useful in monitoring the position of P_4 (but is reliable only at a chosen temperature; use $60^{o}F$). When the compensation is done, step (5) is repeated.

(11) Now conduct a temperature test. First, cool the oven to about $50^{o}F$ and allow the circuit to stabilize approximately. Then raise the temperature to $60^{o}F$ and allow the circuit to become well stabilized. Take a voltage reading. Now raise the oven temperature to $90^{o}F$ and obtain another stabilized reading. Note the size and direction of the voltage drift.

(12) Make a trial adjustment of potentiometer P_4 according to the amount of voltage drift observed. The direction in which P_4 is

initially turned is not important, however, note the direction used. The results of the next trial run will show if it is the correct direction to use.

(13) Restabilize the circuit to 60°F as in step (11). Note the voltage reading. The amount and direction of the voltage change (from the previous 60°F reading) will correspond to the amount and direction of change of P_4. Complete the trial as in step (11).

(14) The information obtained from step (13) will allow an intelligent guess to be made as to the amount and direction of change in P_4 required to bring the width modulator closer to being perfectly temperature compensated. By monitoring the voltage as P_4 is adjusted, the desired adjustment can be closely obtained. This trial and error procedure is continued until the voltage readings at 60°F and 90°F agree with each other as well as possible. Perfect agreement (within 1 mv) can be obtained, but a difference of up to 3 mv is acceptable.

(15) If the situation should occur where there is no adjustment left in P_4, there are two possible solutions.

(a) Connect a resistor in parallel with the resistor joining P_4 with the tunnel diode input (if resistor is soldered into circuit, beware of destroying the tunnel diode with heat; use a heat sink).

(b) If solution (a) produces the wrong voltage change, then remove the parallel resistor and change the position of the shorting bar as indicated in Fig. 5.32. This should make the desired compensation now possible.

(16) After the temperature compensation is completed, repeat the steps (5) through (8). Step (9) can also be checked.

III. OPERATING THE MULTIPLIER

Turn on the multiplier and allow it to warm up for at least 5 minutes. If the multiplier has been previously balanced procede with step (17). (If in doubt, check the balance by repeating steps (6), (7), and (9).

(17) With no inputs connected, adjust P_5 and P_6 (Fig. 5.34) for an exact zero voltage output.

(18) Apply +10 volts D.C. to the x and the y inputs. Adjust P_7 (Fig. 5.35) and/or P_{11} (Fig. 5.36) to produce a -10 volt output voltage at the multiplier output. Remove inputs and check the zero reading. Repeat (17) if necessary.

(19) Apply -10 volts D.C. to the x and the y inputs. If the multiplier output is not -10 volts, adjust P_7 and/or P_{11} such that the output voltage is brought half way toward the previous reading (ie. -10 volts). Remove inputs and check the zero.

(20) Repeat the above procedure for: (x=10, y=-10), (x=-10, y=10). Note, the desired voltage is now +10 volts.

(21) The x and y gain controls (P_{11} and P_7) are adjusted until the best compromise is achieved. If the desired accuracy cannot be obtained, check steps (6) through (9).

(22) If accuracy is still poor, perform the steps (6) and (7) with a $\pm$10 volt D.C. input and D.V.M. instead of a sine wave signal and oscilloscope.

(23) Once desired accuracy is achieved only periodic checking of the zero level will be required. Steps (18) to (21) need not be done each time the multiplier is used unless extreme accuracy is needed.